

GIGABYTE GA-M57SLI-S4 Schematics

Revision:2.03

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	PROCESSOR HT INTERFACE
05	PROCESSOR DDR INTERFACE
06	PROCESSOR DDR INTERFACE
07	PROCESSOR CONTROL & DEBUG
08	DIMM A0,B0
09	DIMM A1,B1
10	DIMM TERMINATION
11	MCP55 HT/CLK
12	MCP55 PCIE X16
13	MCP55 PCIE X8 X1
14	MCP55 PCI
15	MCP55 SATA , IDE
16	MCP55 AUDIO , USB , MISC
17	MCP55 DUAL RGMII
18	MCP55 PWR/GND
19	MCP55 DECOUPLING
20	PCI EXPRESS X16 SLOT
21	PCI EXPRESS X8 SLOT
22	PCI EXPRESS X1 SLOT1,2,3
23	PCI 1,2 SLOT
24	CODEC 883
25	AUDIO JACK, L_OUT, F_AUDIO

SHEET

TITLE

26	IDE1/FDD
27	KB_MS/FUSEVCC
28	VCORE POWER
29	VCC12_HT,VCCA25,VCC15,PLL POWER
30	PWR SEQUENCE PWR
31	DDR18 , DDRVTT , 5VDUAL
32	ATX POWER CONNCTOR,VCC15
33	DUAL BIOS
34	FRONT PANEL
35	ITE 8716F (GB)
36	FAN/HW MONITOR
37	F_USB1/F_USB2/F_USB3 CONNECTOR
38	COMA , LPT , TPM , R_USB
39	MARVELL 1116 RGMII PHY -A
40	TI TSB43AB23 1394A
41	CURRENT_OUT
42	
43	
44	

GIGABYTE CORP.

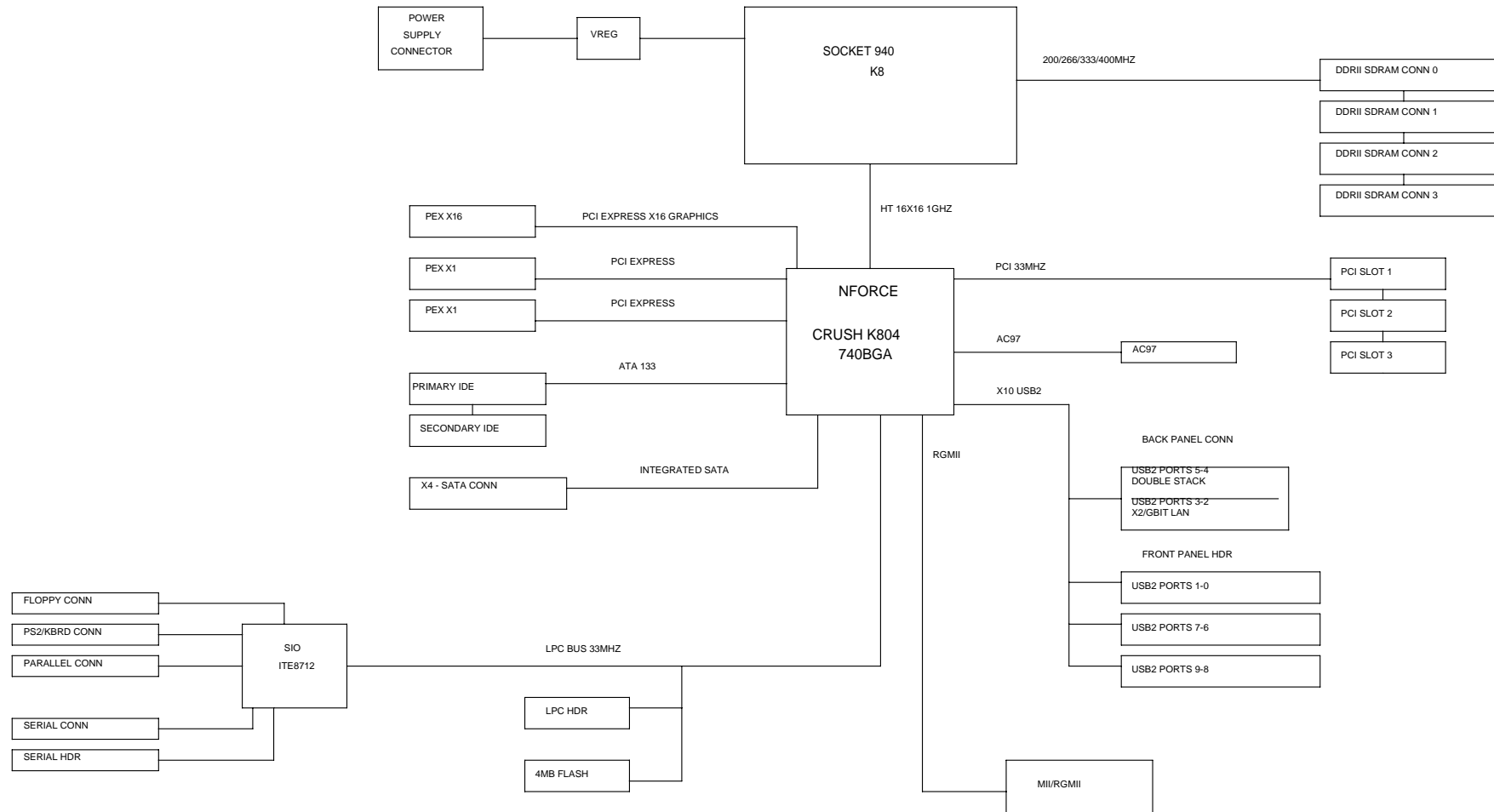
Title			
BLOCK DIAGRAM			
Size	Document Number	Rev	
Custom	GA-M57SLI-S4	2.03	
Date:	Friday, March 09, 2007	Sheet	1 of 41

Component value change history

Date	Change Item	Reason
REV0.1 2006/03/27	First release.	
2006/11/16	REV2.01	
	change codec from ALC883 to ALC888	
	remove CR10	
	change CR32 from 220ohm to 2.2ohm	
	CR45 change to 470pf	
	CBC17,CBC18,CBC21 change to 0.1uf	
2006/12/05	REV2.01	
	remove C66 R85	
2006/12/12	REV2.02	
	DL1,DL2,DL3,DL4 footprint-->CHOCK06U-40A_1PDL-2	
	L1,L4, footprint-->CHOCK2U-20A_SQ-2	
	L2,L3, footprint-->CHOCK08U-15A_1P-1	
2006/12/26	REV2.02	
	CBC50,CBC51,CBC52,CBC53:4.7u/8/X5R/25V/K-->4.7u/8/X5R/10V/K	
	REV2.03	
2007/01/26	Q48 改 TO252	
	M57SLI-S4 rev 2.03	
2007/03/08	All solid polymer capacitors change to electrolytic capacitors	

[illegible]

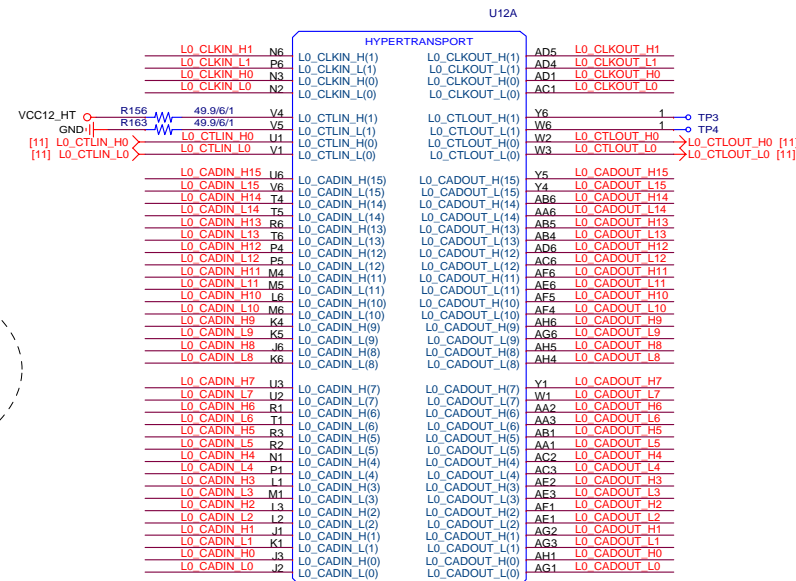
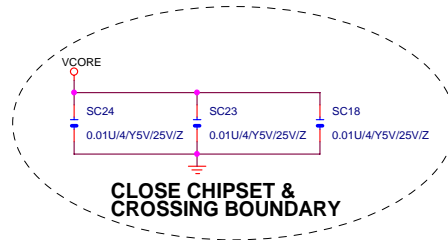
BLOCK DIAGRAM



GIGABYTE CORP.

Title				
BLOCK DIAGRAM				
Size	Document Number			Rev
Custom	GA-M57SLI-S4			2.03
Date:	Friday, March 09, 2007	Sheet	3 of 41	

L0_CADIN_L[0..15] <L0_CADIN_L[0..15] [11]
L0_CADIN_H[0..15] <L0_CADIN_H[0..15] [11]
L0_CLKIN_L[0..1] <L0_CLKIN_L[0..1] [11]
L0_CLKIN_H[0..1] <L0_CLKIN_H[0..1] [11]
L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] [11]
L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] [11]
L0_CLKOUT_L[0..1] <L0_CLKOUT_L[0..1] [11]
L0_CLKOUT_H[0..1] <L0_CLKOUT_H[0..1] [11]

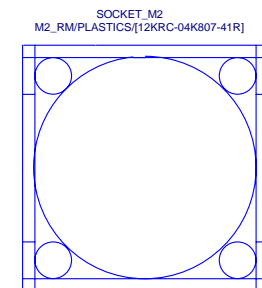


```
CPU_VDDA_RUN = VDDA25
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT
```

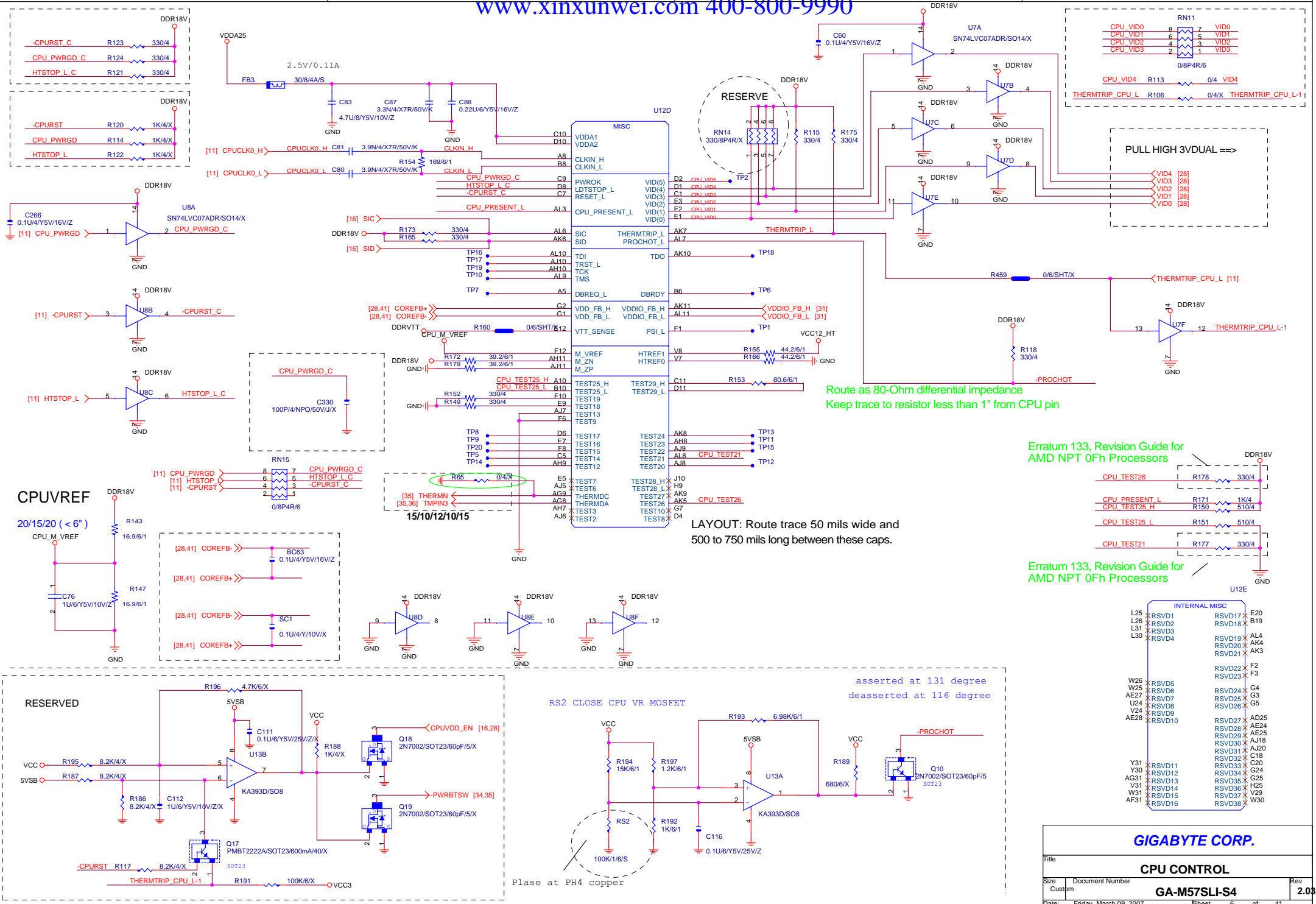
CPU_VDD_RUN = VCORE

VLDT_RUN = VCC12_HT

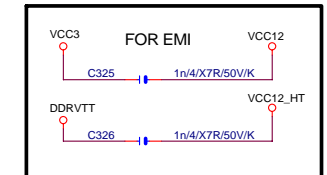
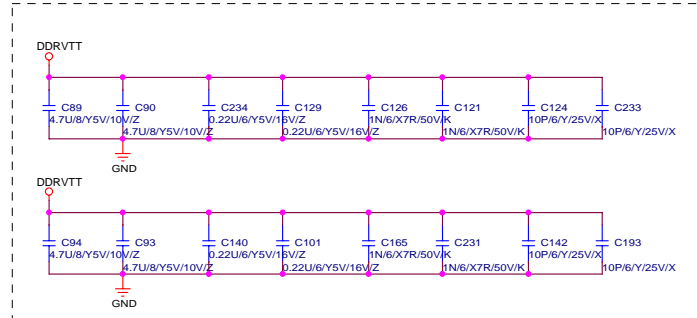
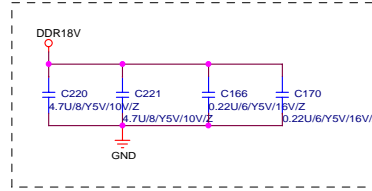
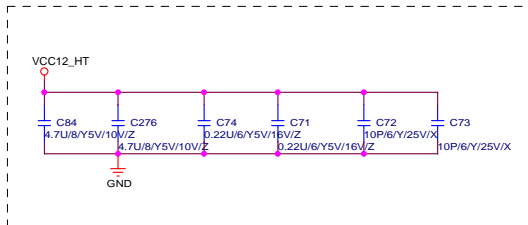
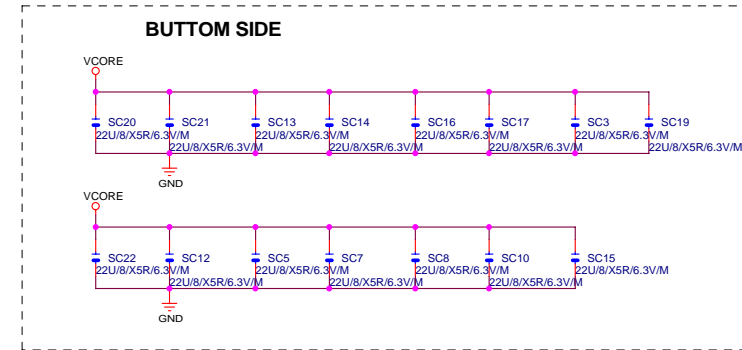
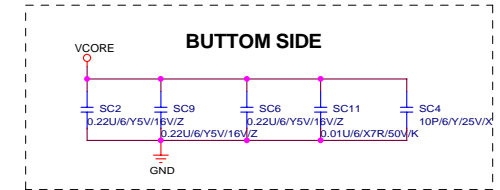
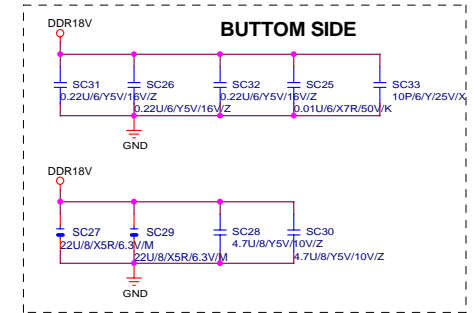
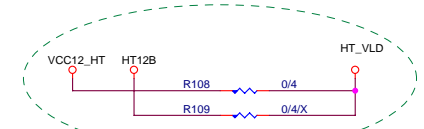
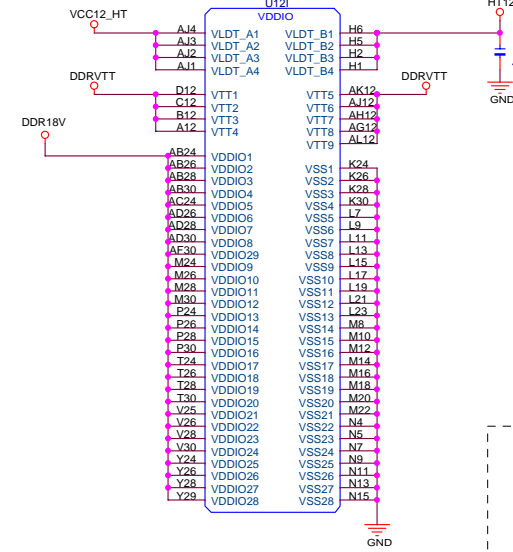
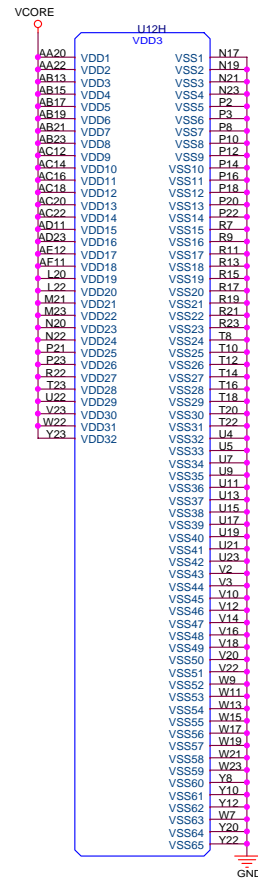
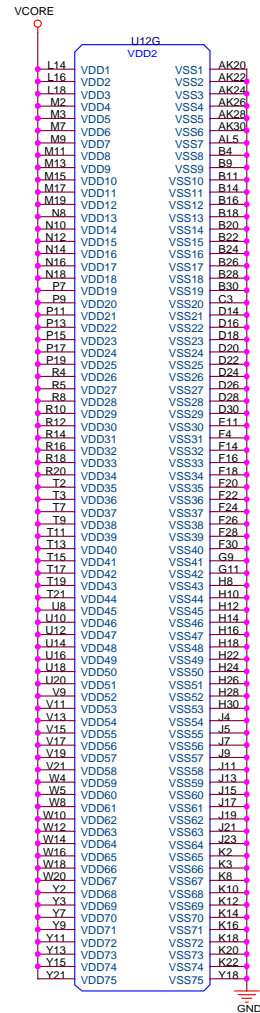
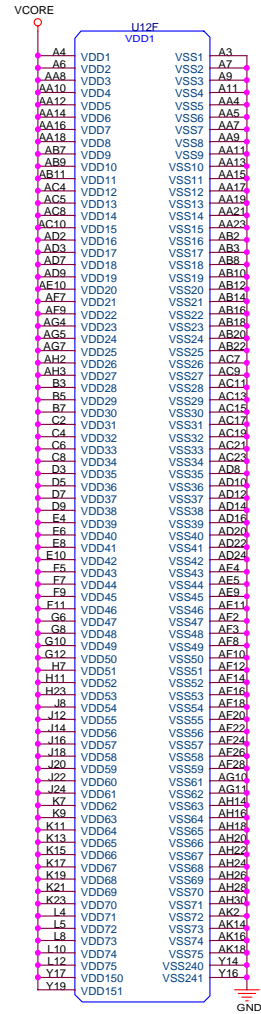
```
VLDT_A = VCC12_HT
VLDT_B = HT12B
```



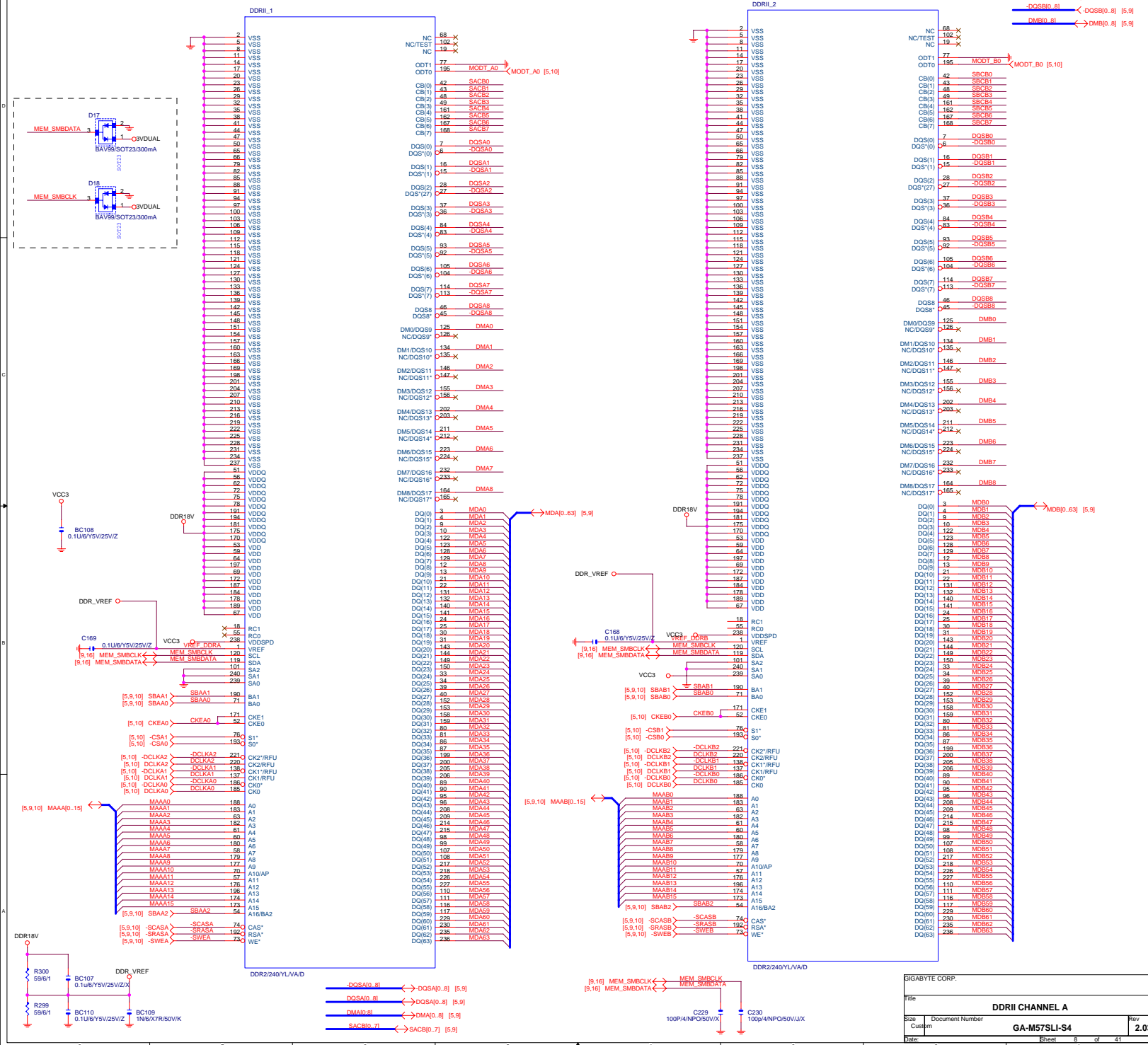


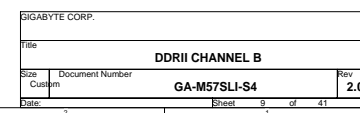


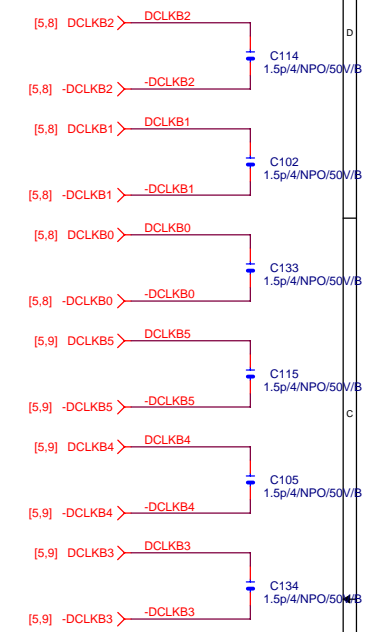
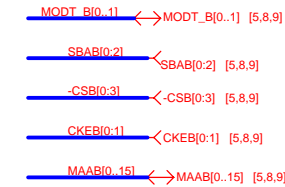
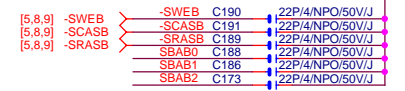
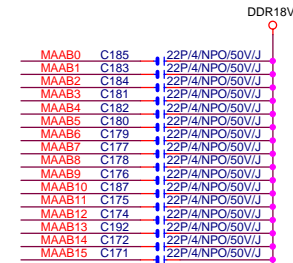
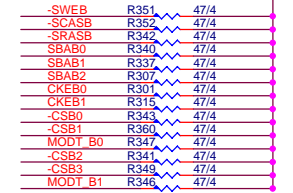
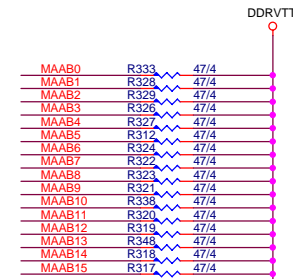
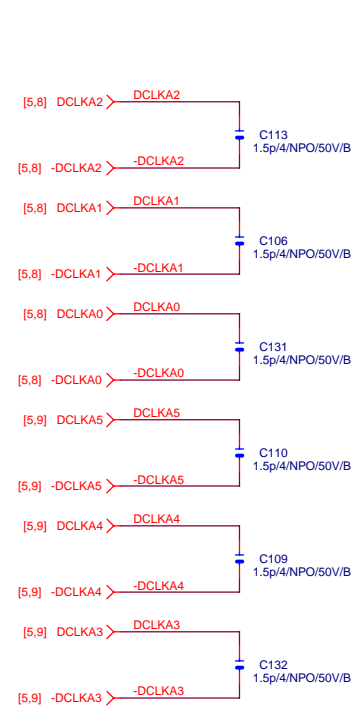
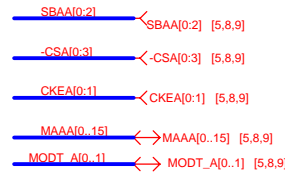
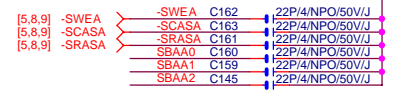
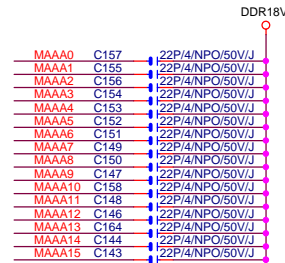
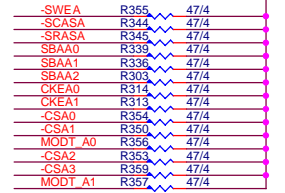
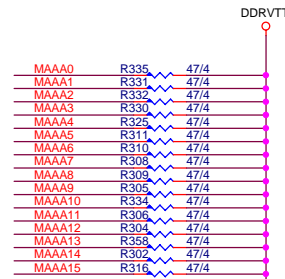
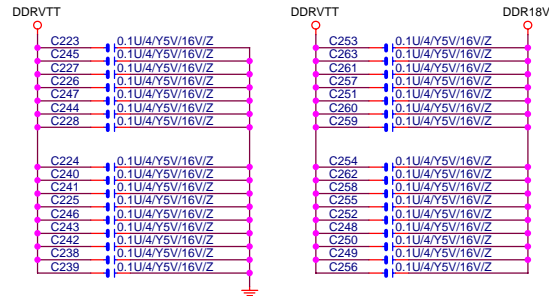
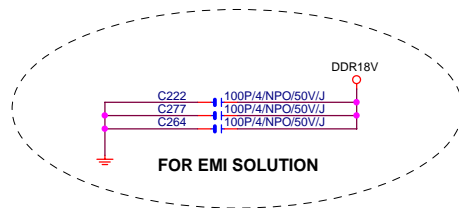
VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.



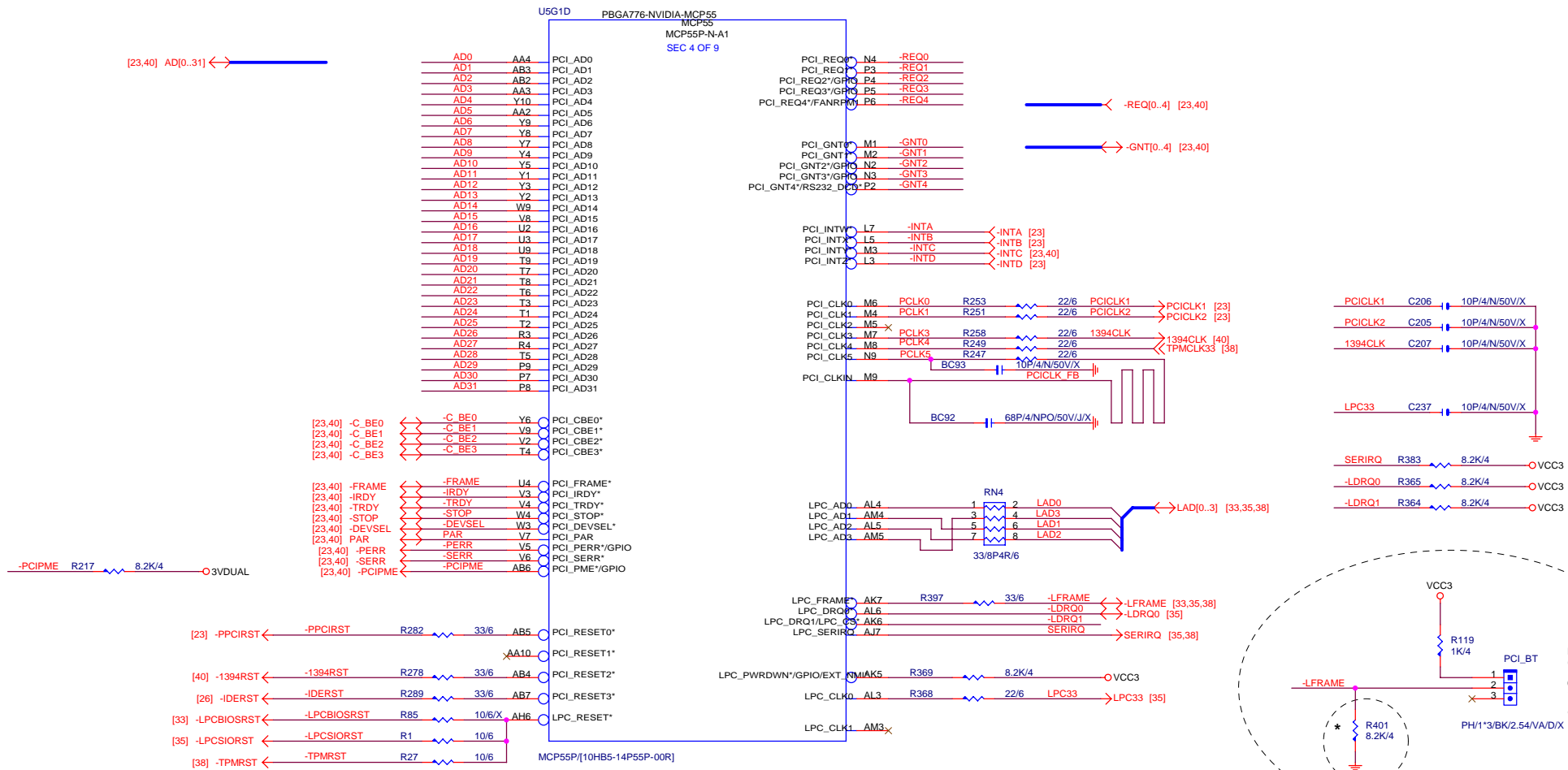
GIGABYTE CORP.			
CPU POWER & GND			
Title	Document Number	Rev	
Size	Custpm	GA-M57SLI-S4	2.08
Date:	Friday, March 09, 2007	Sheet	7 of 41







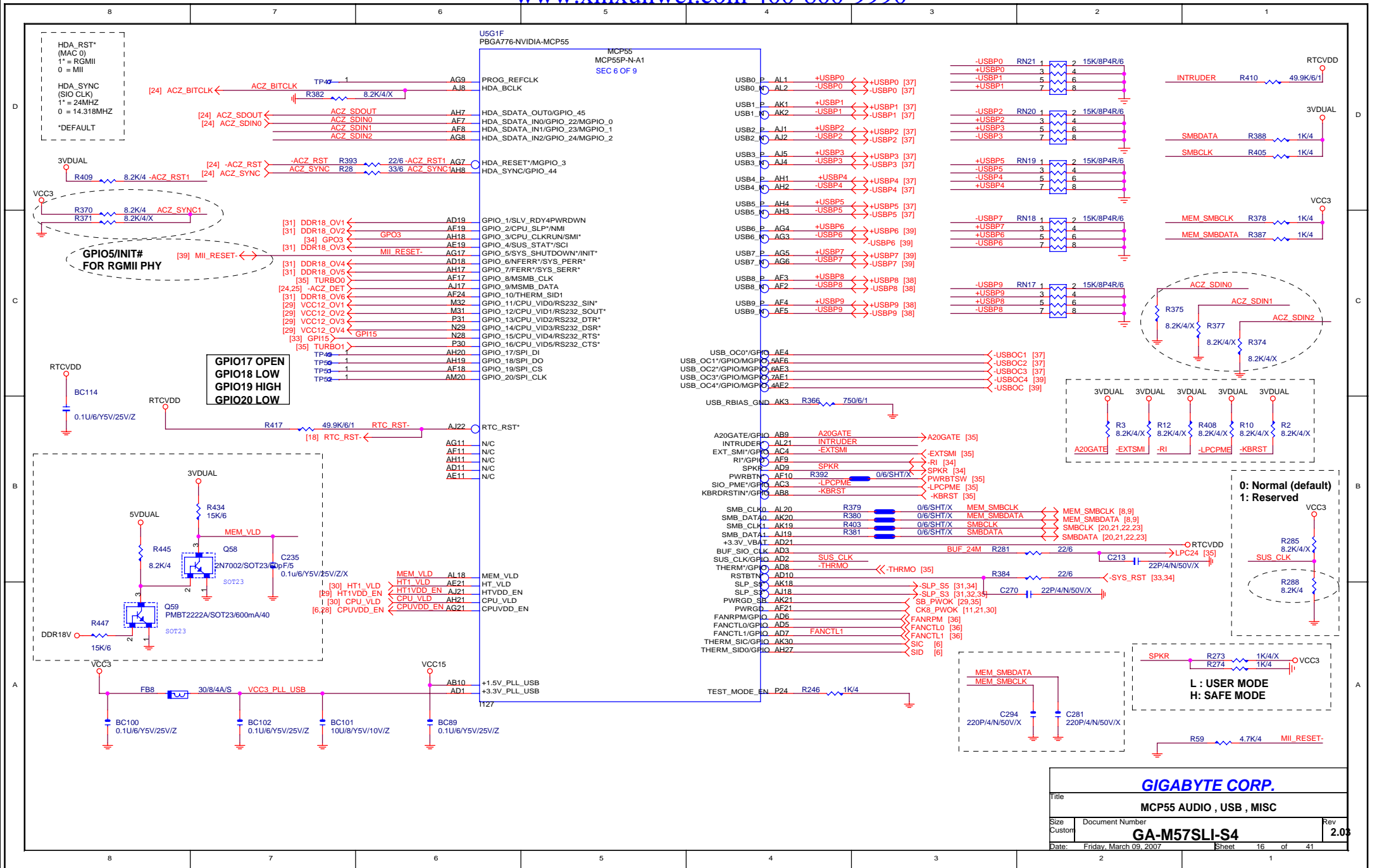
Size Custom	Document Number GA-M57SLI-S4	Rev 2.03
Date: Friday, March 09, 2007	Sheet 11 of 41	

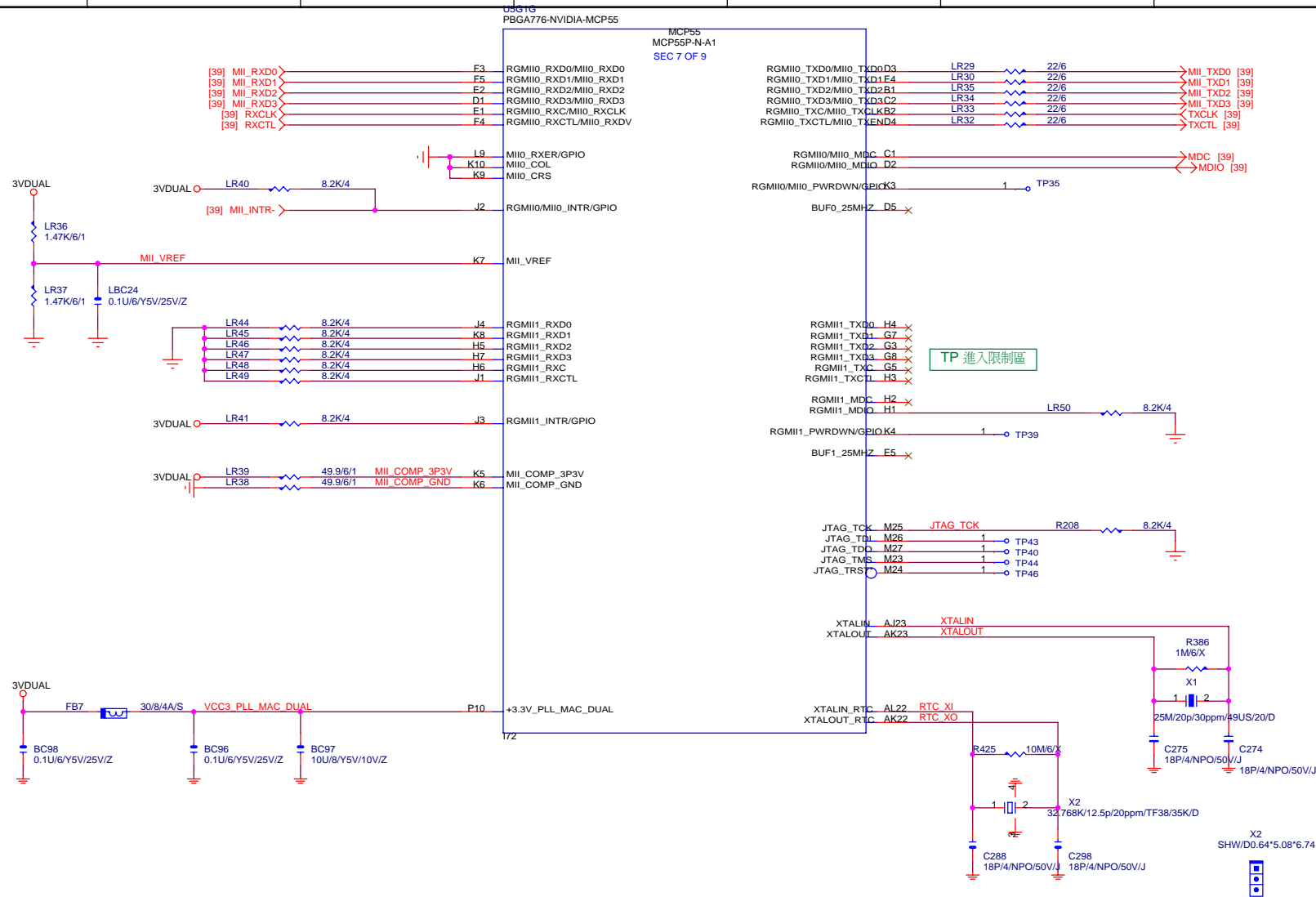


GIGABYTE CORP.

MCP55 PCI

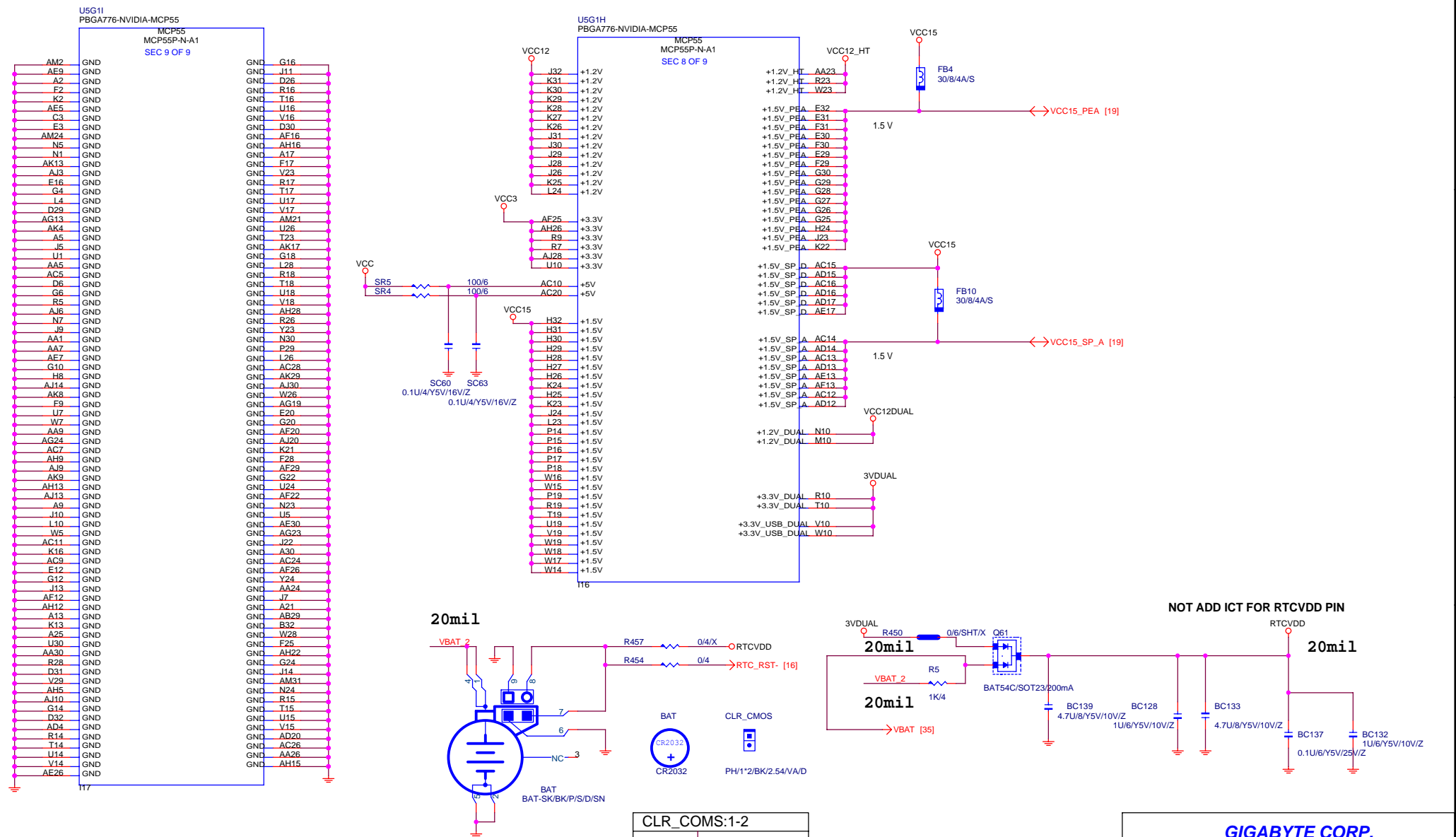
Title		
MCP55 PCI		
Size	Document Number	Rev
Custom	GA-M57SLI-S4	2.03
Date:	Friday, March 09, 2007	Sheet 14 of 41





GIGABYTE CORP.

Title			MCP55 DUAL RGMII	
Size	Document Number		Rev	
Custom	GA-M57SLI-S4		2.03	
Date:	Friday, March 09, 2007		Sheet	17 of 41



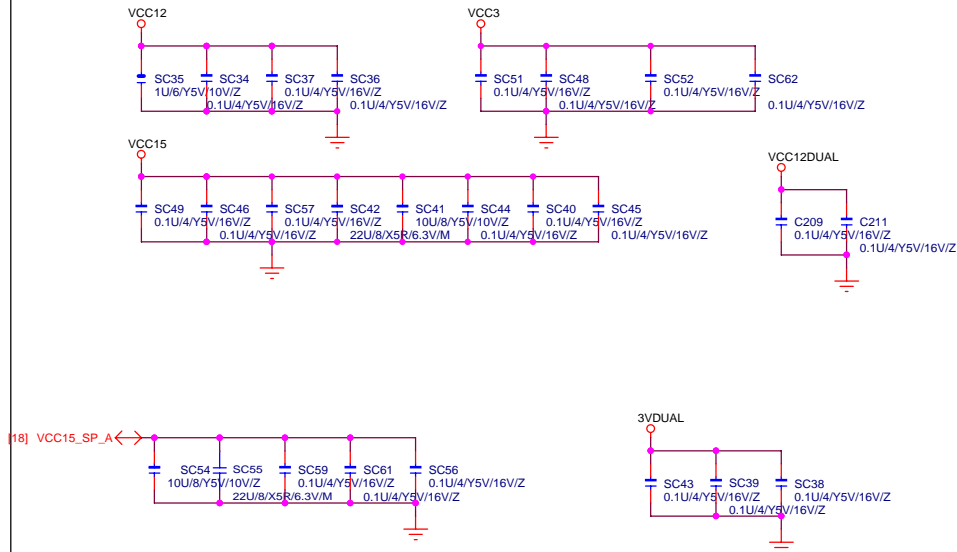
CLR_COMS:1-2	
SHORT	CLEAR CMOS
OPEN	NORMAL

GIGABYTE CORP.

MCP55 PWR/GND

Size Custom	Document Number GA-M57SLI-S4	Rev 2.0
Date:	Friday, March 09, 2007	Sheet 18 of 41

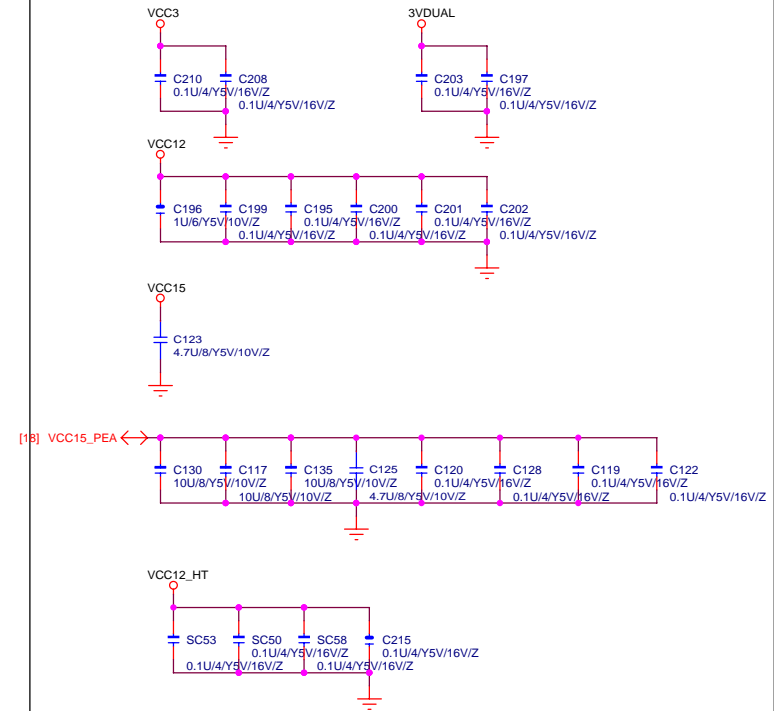
MCP55 BACK SIDE DECOUPLING



MCP55 INTERNAL PULL-UP/PULL-DOWN

PIN	VOLTAGE
A20GATE/GPIO	+3.3V
EXT_SMI*/GPIO	+3.3V_DUAL
HDA_SDATA_IN0/GPIO_22/MGPIO_0	+3.3V_DUAL/GND
HDA_SDATA_IN1/GPIO_23/MGPIO_1	+3.3V_DUAL/GND
HDA_SDATA_IN2/GPIO_24/MGPIO_2	+3.3V_DUAL/GND
HDA_SDATA_OUT/GPIO_45	+3.3V_DUAL/GND
JTAG_TDI	+3.3V
JTAG_TMS	+3.3V
JTAG_TRST*	GND
KBRDRSTIN*/GPIO	+3.3V
PE_WAKE*	+3.3V_DUAL
SIO_PME*/GPIO	+3.3V_DUAL
THERM*/GPIO	+3.3V

MCP55 TOP SIDE DECOUPLING

**GIGABYTE CORP.**

Title

MCP55 DECOUPLING

Size
Custom

Document Number

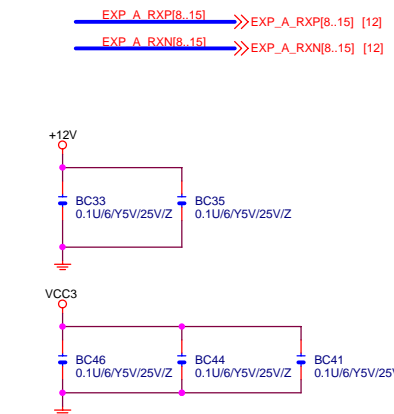
GA-M57SLI-S4

Rev

2.03

Date: Friday, March 09, 2007

Sheet 19 of 41

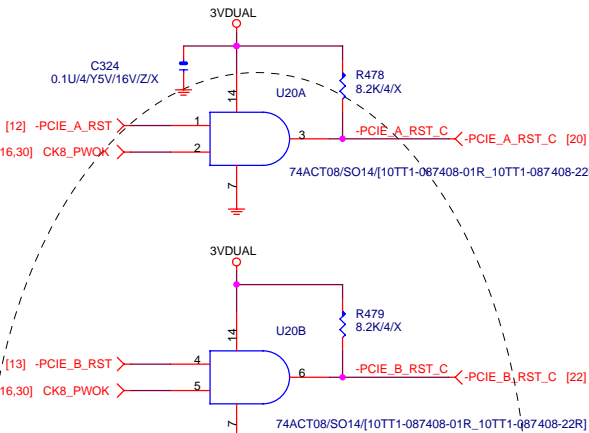


Title			
PCI EXPRESS X 16			
Size Custom	Document Number	GA-M57SLI-S4	Rev 2.0
Date:	Friday, March 09, 2007	Sheet	20 of 41

EXP_B_TXP0	C17	0.1u/4/Y5V/16V/Z	EXP_B_TXP0C
EXP_B_TXN0	C21	0.1u/4/Y5V/16V/Z	EXP_B_TXN0C
EXP_B_TXP1	C30	0.1u/4/Y5V/16V/Z	EXP_B_TXP1C
EXP_B_TXN1	C31	0.1u/4/Y5V/16V/Z	EXP_B_TXN1C
EXP_B_TXP2	C34	0.1u/4/Y5V/16V/Z	EXP_B_TXP2C
EXP_B_TXN2	C35	0.1u/4/Y5V/16V/Z	EXP_B_TXN2C
EXP_B_TXP3	C38	0.1u/4/Y5V/16V/Z	EXP_B_TXP3C
EXP_B_TXN3	C39	0.1u/4/Y5V/16V/Z	EXP_B_TXN3C
EXP_B_TXP4	C46	0.1u/4/Y5V/16V/Z	EXP_B_TXP4C
EXP_B_TXN4	C49	0.1u/4/Y5V/16V/Z	EXP_B_TXN4C
EXP_B_TXP5	C52	0.1u/4/Y5V/16V/Z	EXP_B_TXP5C
EXP_B_TXN5	C54	0.1u/4/Y5V/16V/Z	EXP_B_TXN5C
EXP_B_TXP6	C56	0.1u/4/Y5V/16V/Z	EXP_B_TXP6C
EXP_B_TXN6	C59	0.1u/4/Y5V/16V/Z	EXP_B_TXN6C
EXP_B_TXP7	C62	0.1u/4/Y5V/16V/Z	EXP_B_TXP7C
EXP_B_TXN7	C64	0.1u/4/Y5V/16V/Z	EXP_B_TXN7C

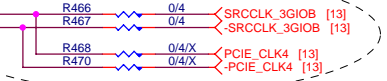
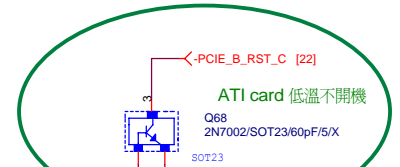
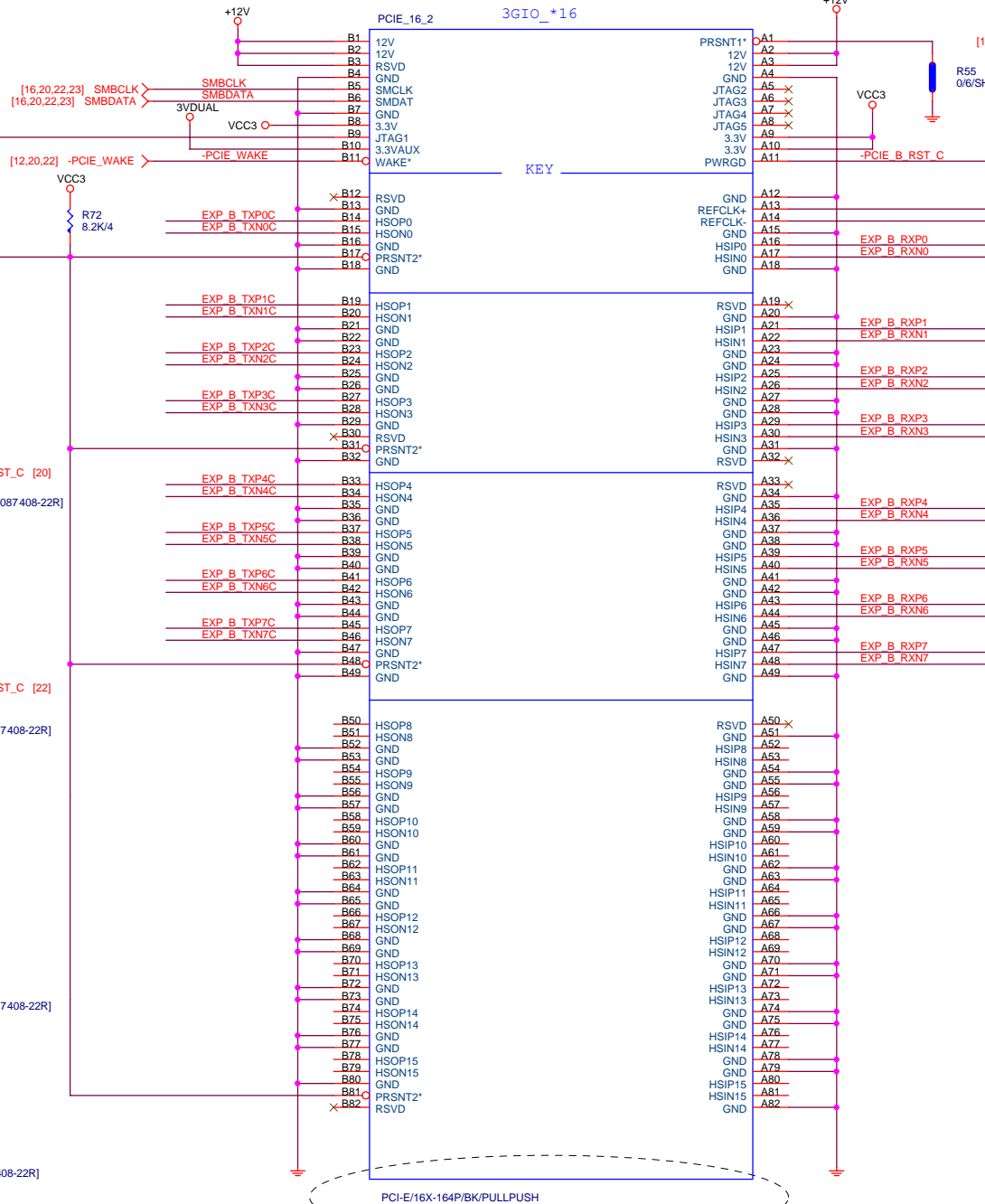
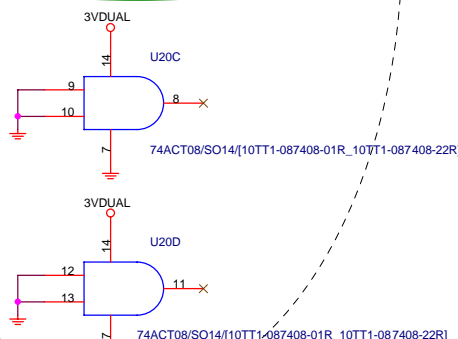
EXP_B_TXP0_71 >>> EXP_B_TXP[0..7] [13]
EXP_B_TXN0_71 >>> EXP_B_TXN[0..7] [13]

[13] PE5_PRSNT- R469 0/4
[13] PE4_PRSNT- R471 0/4/X

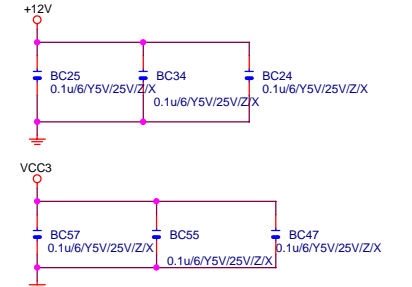
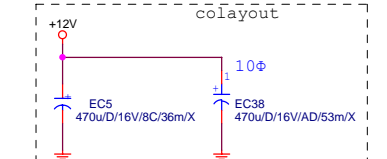
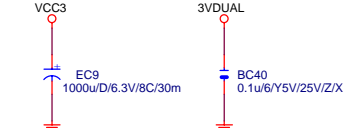
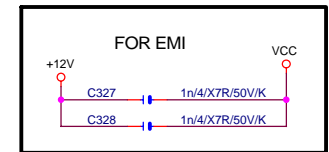


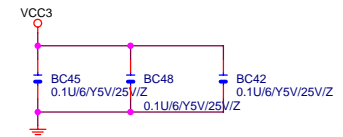
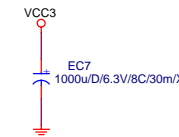
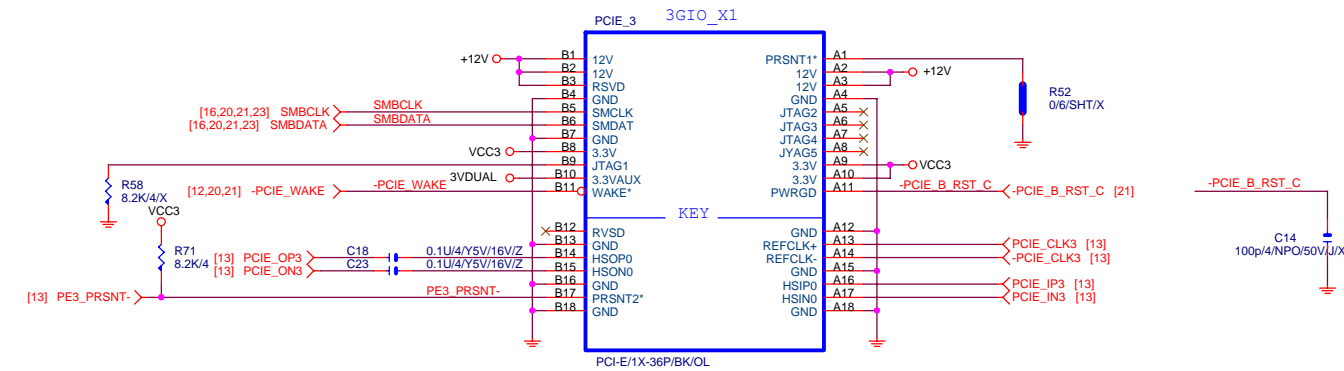
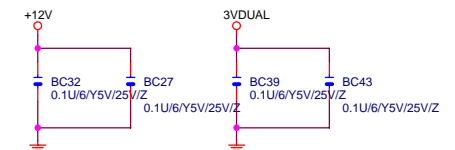
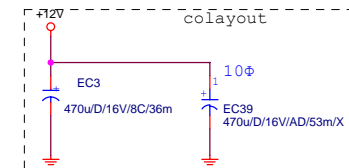
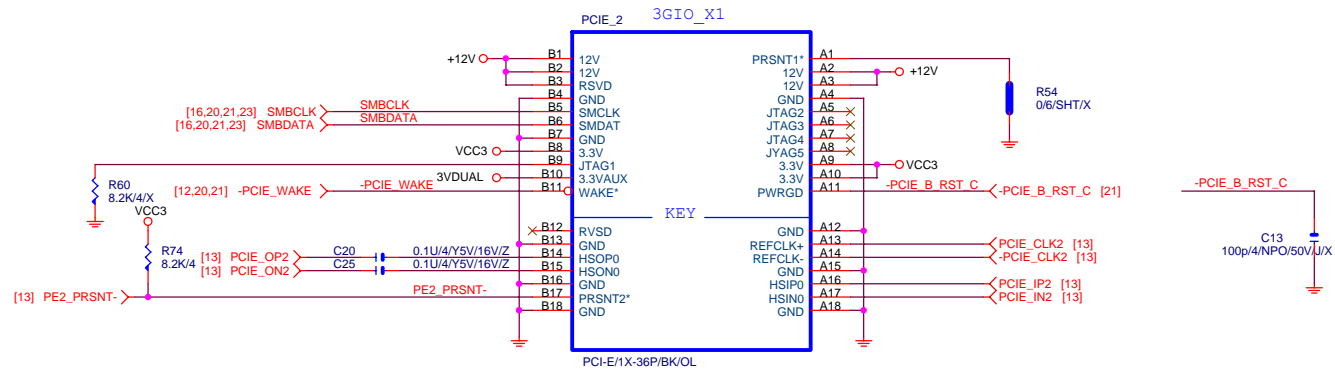
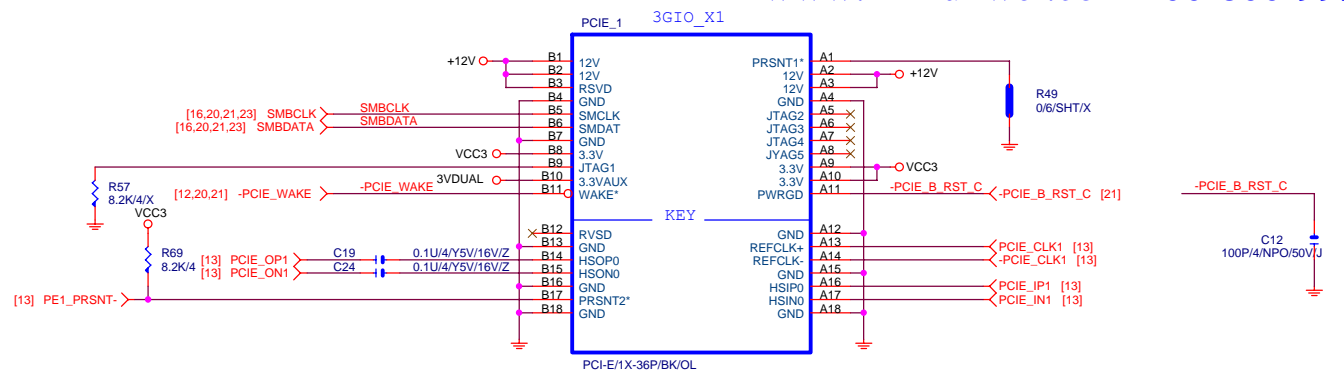
PCIE_A_RST R480 0/4/X PCIE_A_RST_C
PCIE_B_RST R481 0/4/X PCIE_B_RST_C

**VCC3 10% to Core power 90% < 30ms
else, PCIE_RST add 74ACT08**



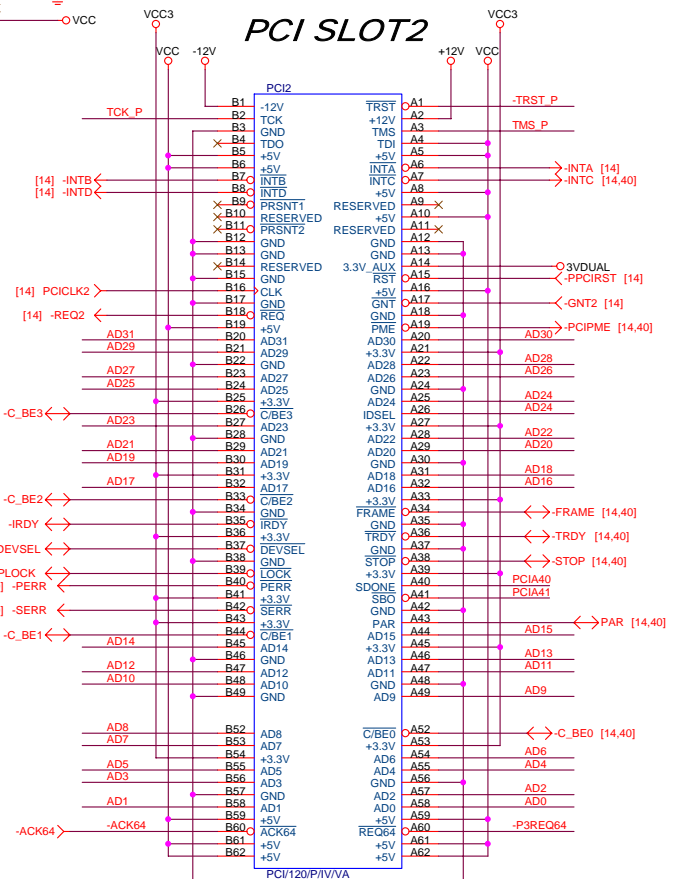
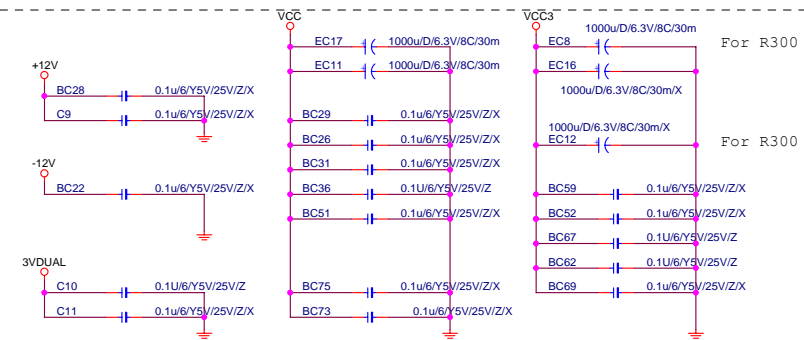
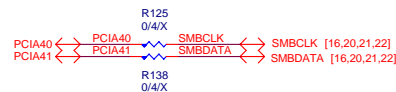
EXP_B_RXP0_71 >>> EXP_B_RXP[0..7] [13]
EXP_B_RXN0_71 >>> EXP_B_RXN[0..7] [13]





GIGABYTE CORP.

Title			
PCI E SLOT 1, 2			
GA-M57SLI-S4			
Size B	Document Number	Rev	2.03
Date:	Friday, March 09, 2007	Sheet	22 of 41

IDSEL(A24)
(A)

VCC3

FOR EMU

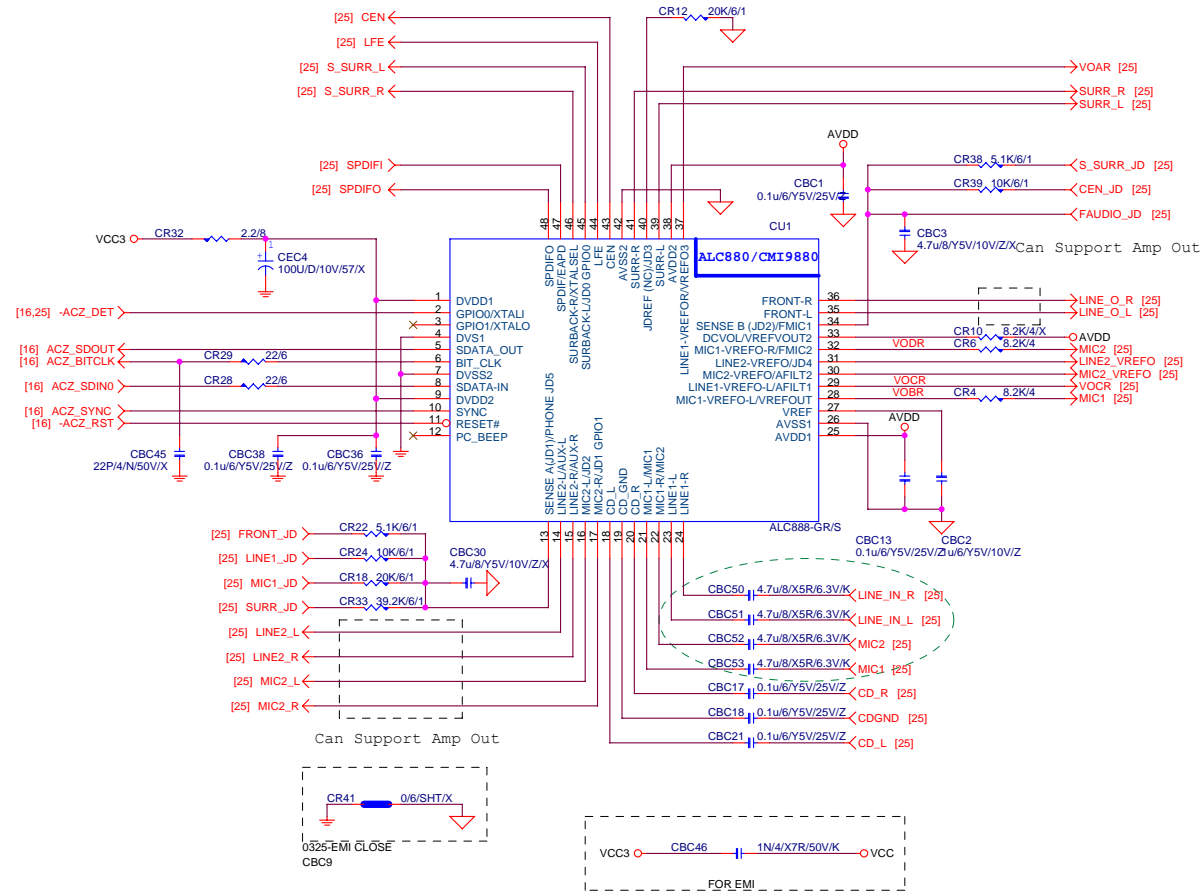
VCC3

BC37

0.1u/6/Y5V/25V/Z

Title			
PCI SLOT 1,2			
Size Custom	Document Number	GA-M57SLI-S4	Rev 2.03
Date:	Friday, March 09, 2007	Sheet	23 of 41

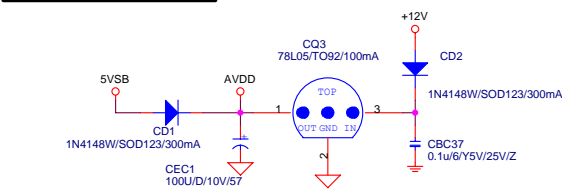
AZALIA CODEC



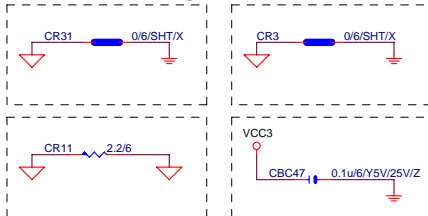
GIGABYTE CORP.

Title			
AZALIA-ALC888			
Size	Document Number	Rev	
Custom	GA-M57SLI-S4	2.03	
Date:	Friday, March 09, 2007	Sheet	24 of 41

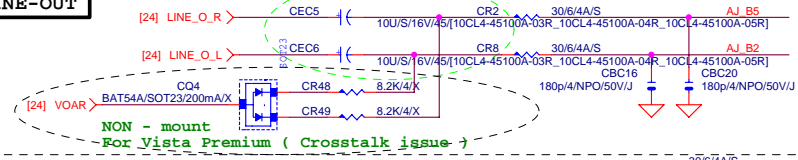
CODEC POWER/EMI PAD



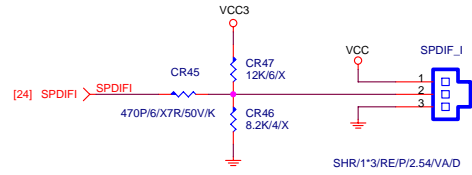
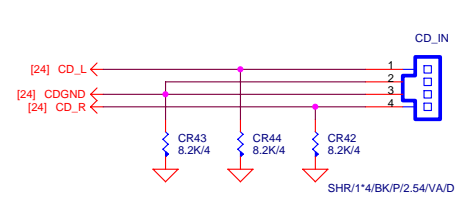
FOR EMI



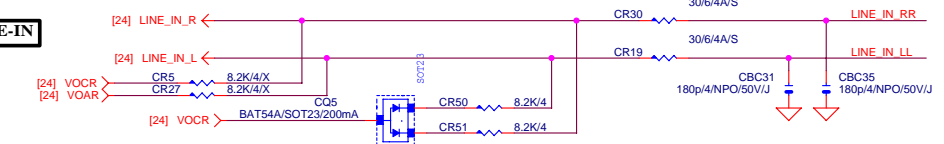
LINE-OUT



CD IN



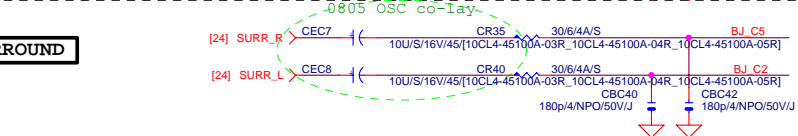
LINE-IN



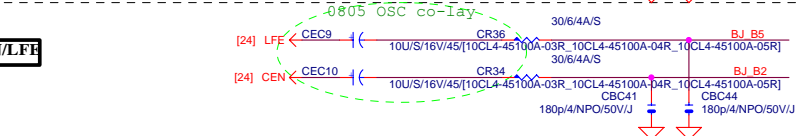
MIC-IN



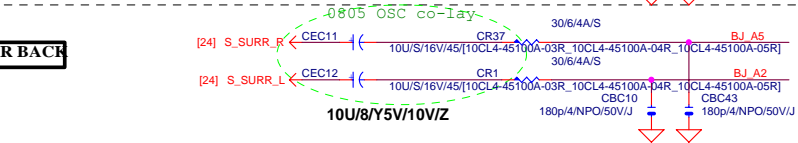
SURROUND



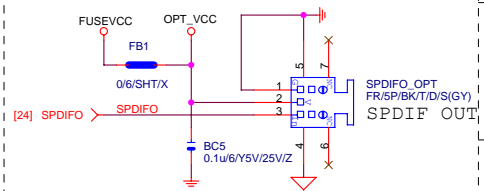
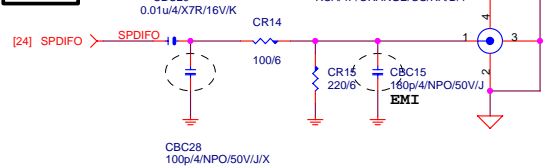
CEN/LFE



SURR BACK

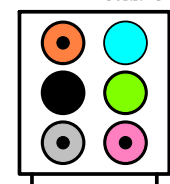


SPDIF

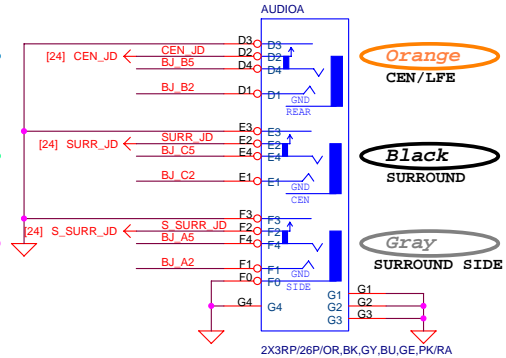
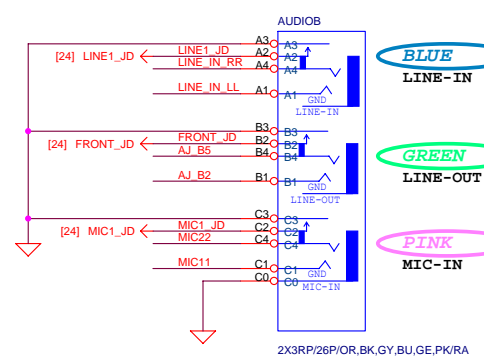
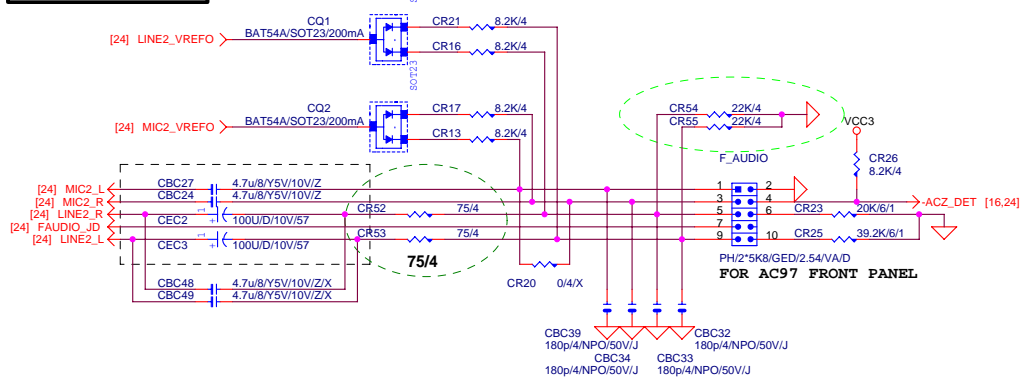


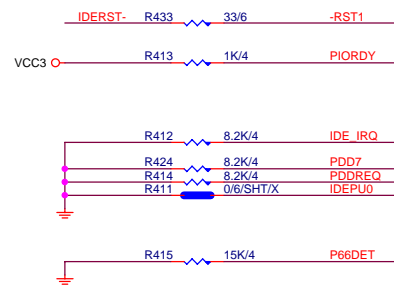
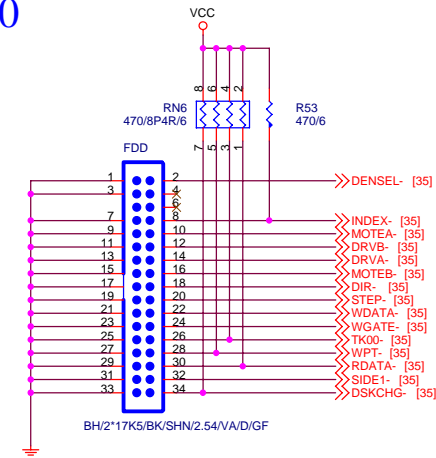
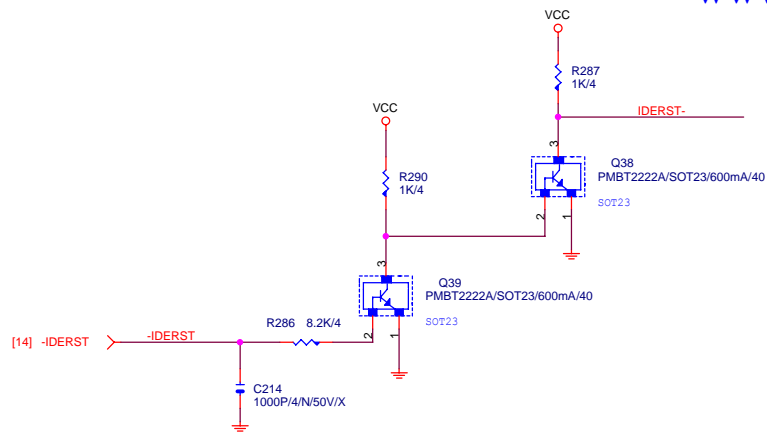
AZALIA JACK

BTX AZALIA CONNECTOR

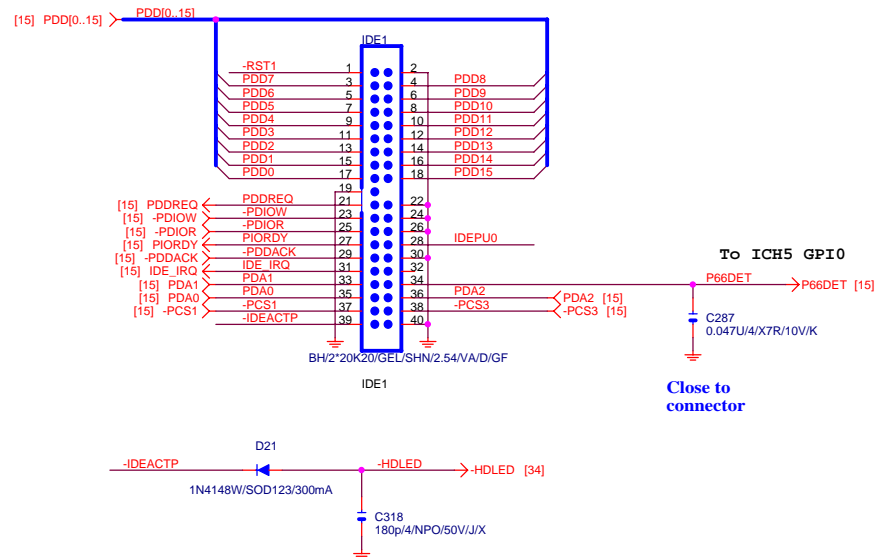


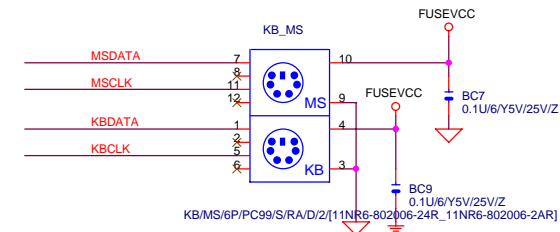
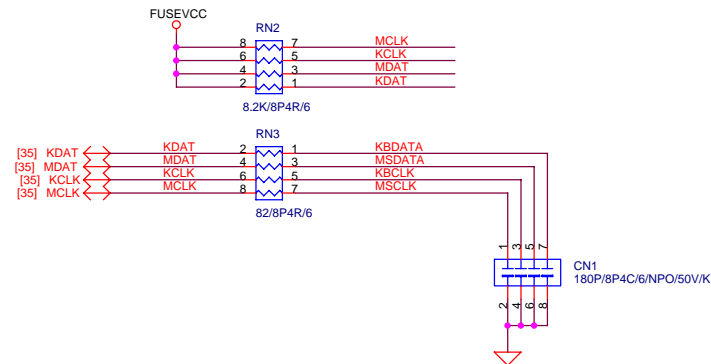
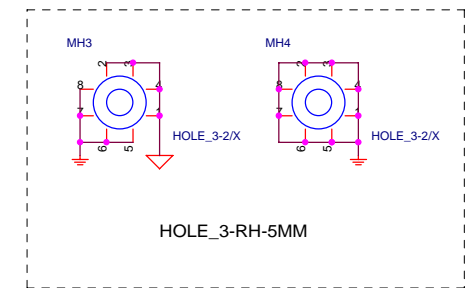
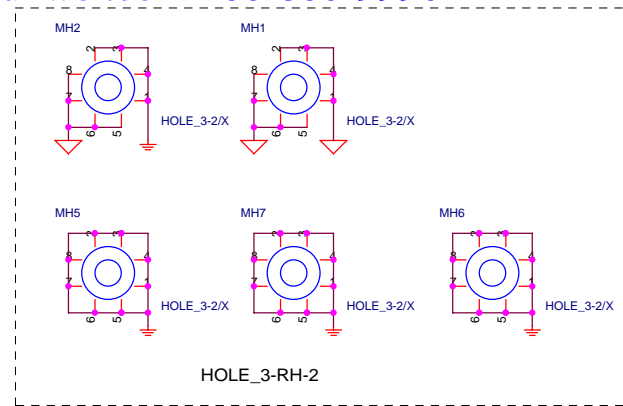
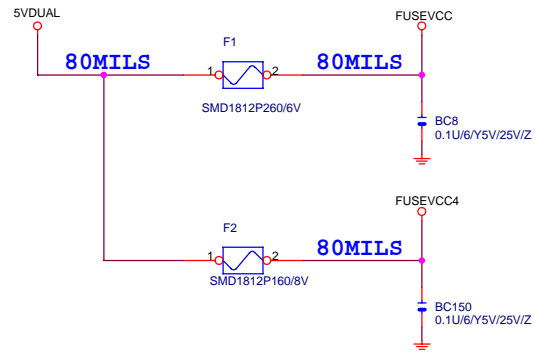
11NR6-403007-21

**AZALIA FRONT PANEL**



PRIMARY IDE CONNECTOR





GIGABYTE CORP.

Title

KB & PS2 MOUSE & IR

Size

Document Number

GA-M57SLI-S4

Rev

2.03

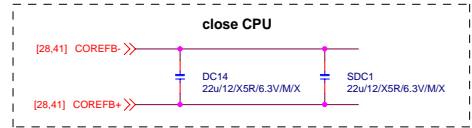
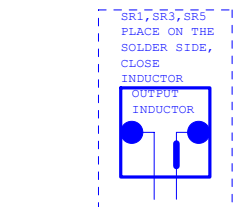
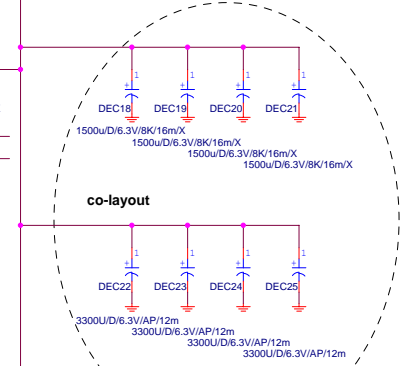
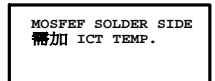
Date:

Sheet

27

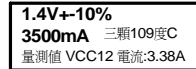
of

41

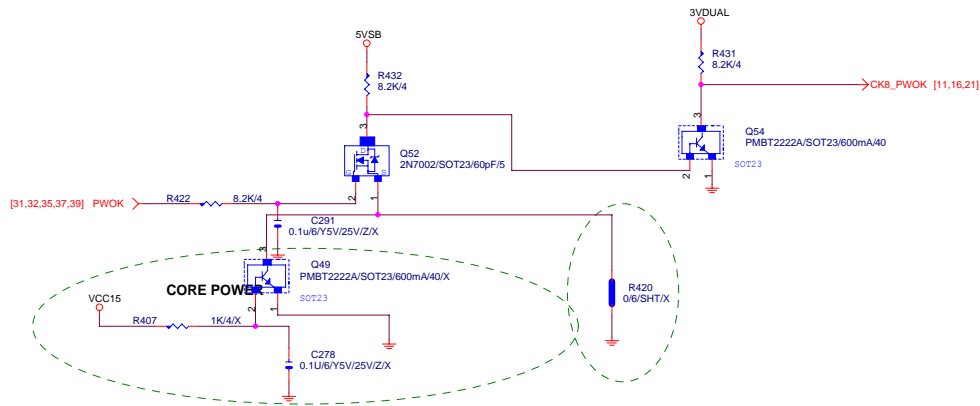
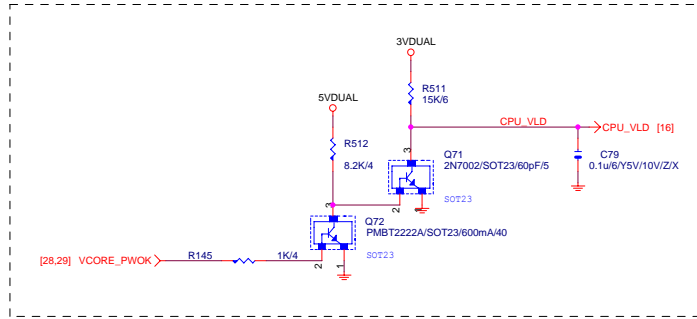
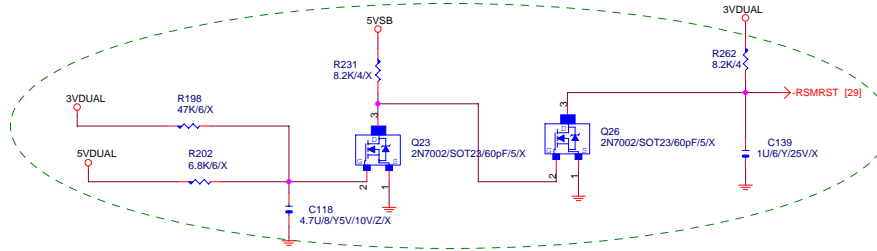
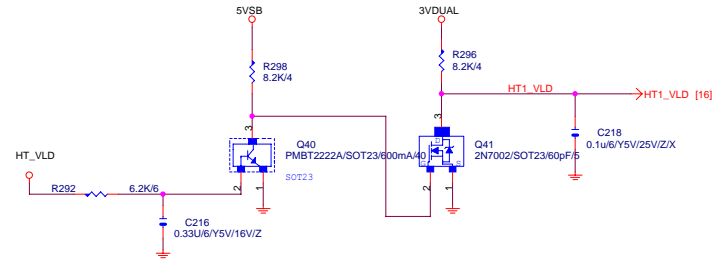


$$1.25(1+12/100)=1.4V$$


CLOSE R418



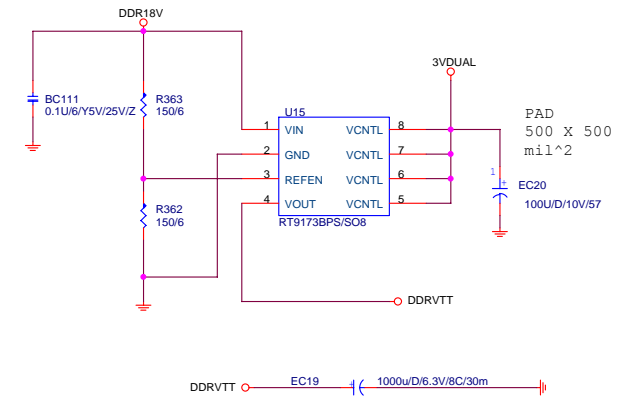
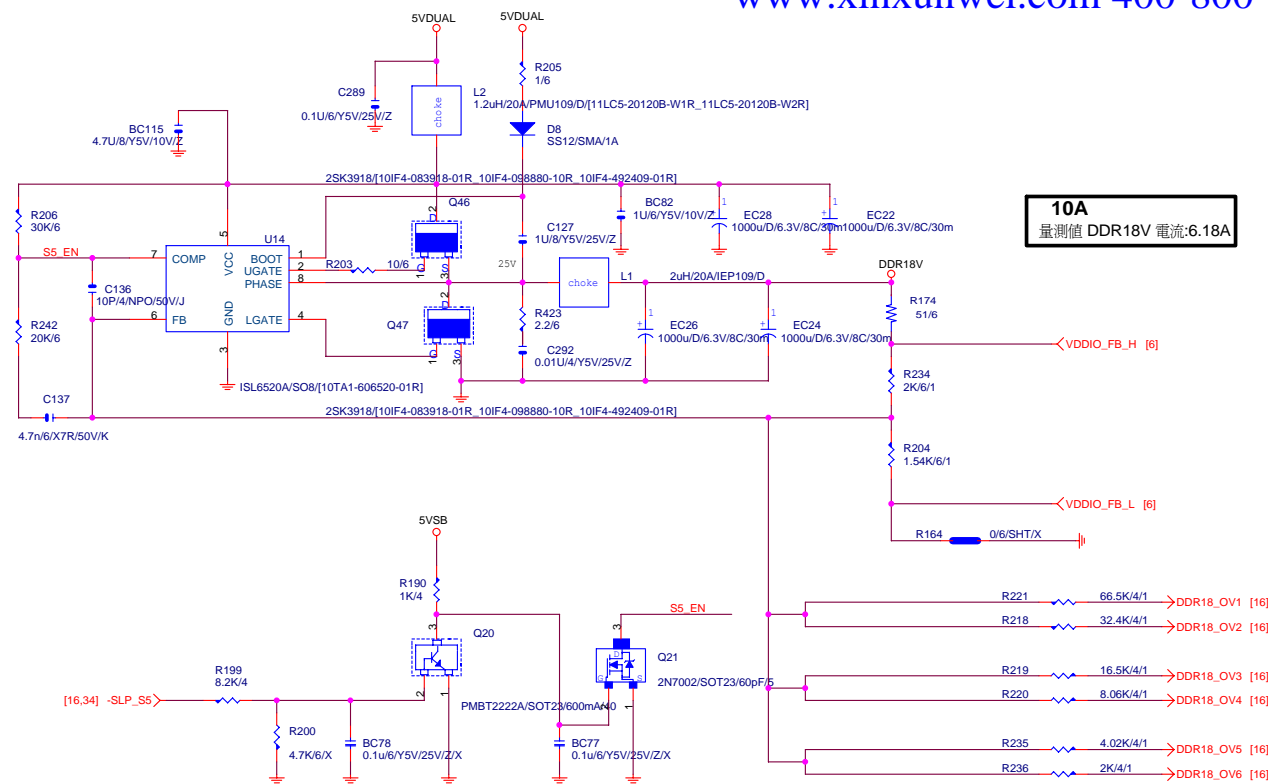
Title				VCC12 HT,VCCA25,PLL POWER			
Size	Document Number						Rev
	GA-M57SLI-S4						2.
Date:	Friday, March 09, 2007			Sheet	29	of	41



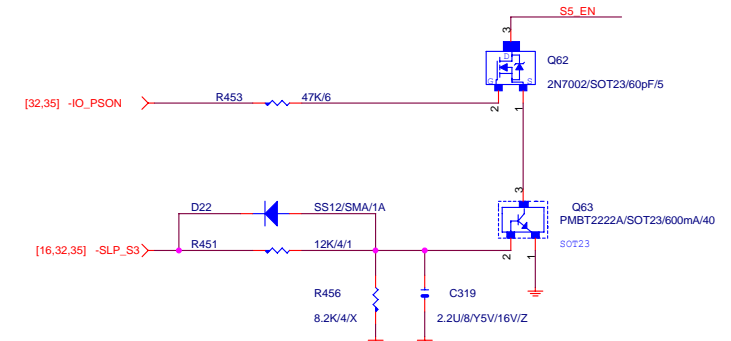
A

B

C



for G3 to G2 status



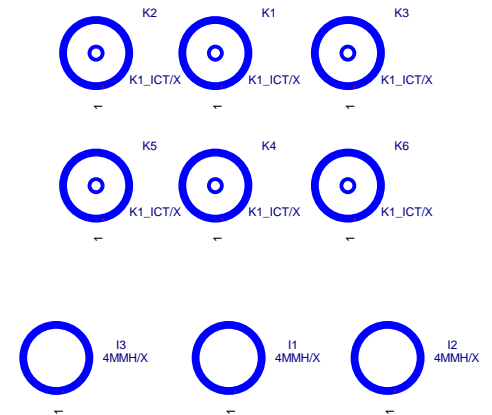
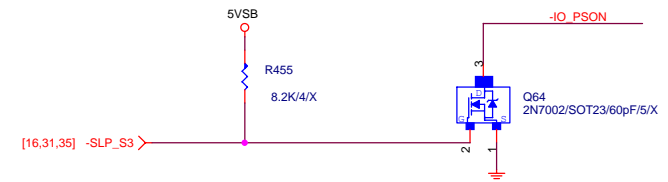
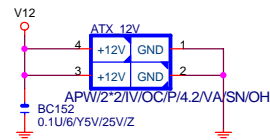
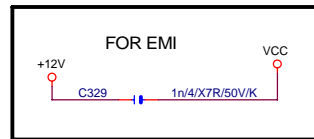
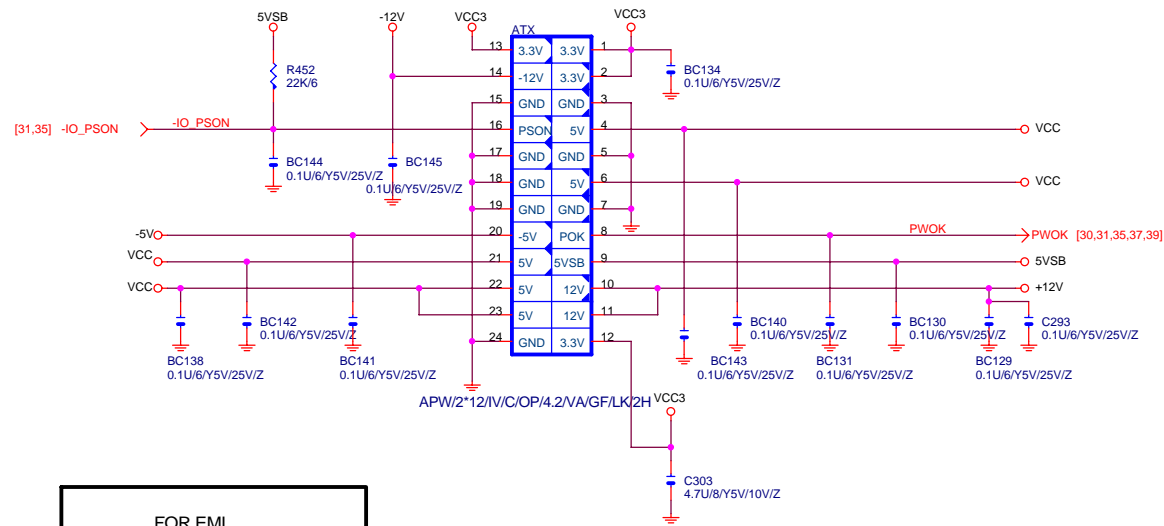
	G2	S5/S4	S3	S1/S0
-SLP_S5	H	L	H	H
-IO_PSON	H	H	H	L
-SLP_S3	H	L	L	H
DDR18V				

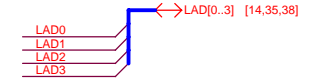
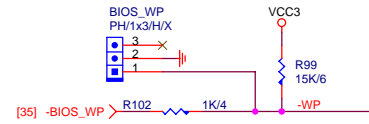
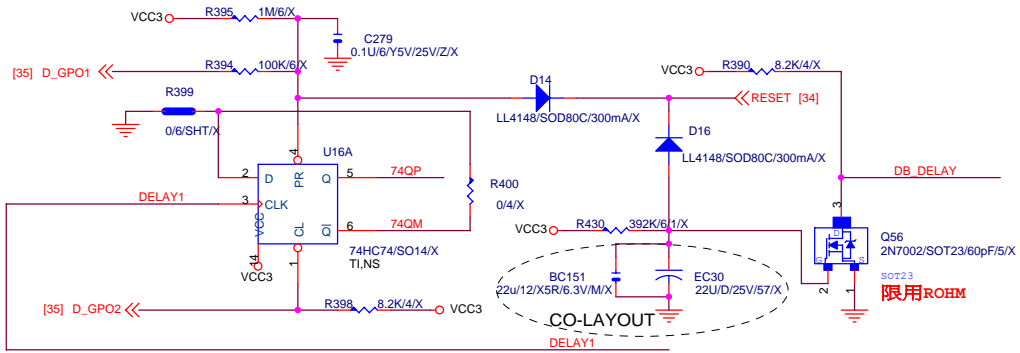
GIGABYTE CORP.

DDR18 , DDRVTT , 5VDUAL

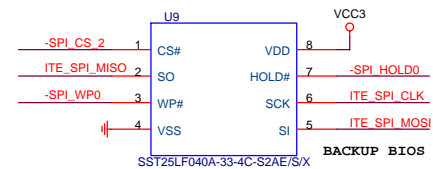
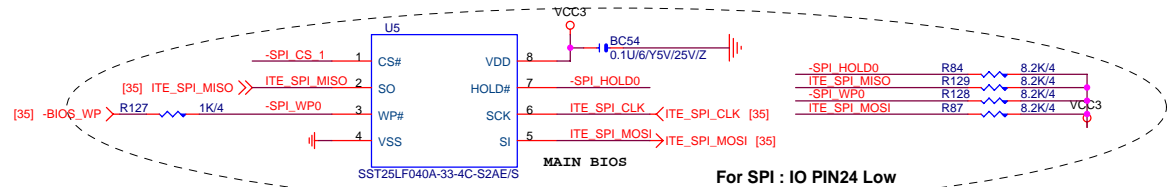
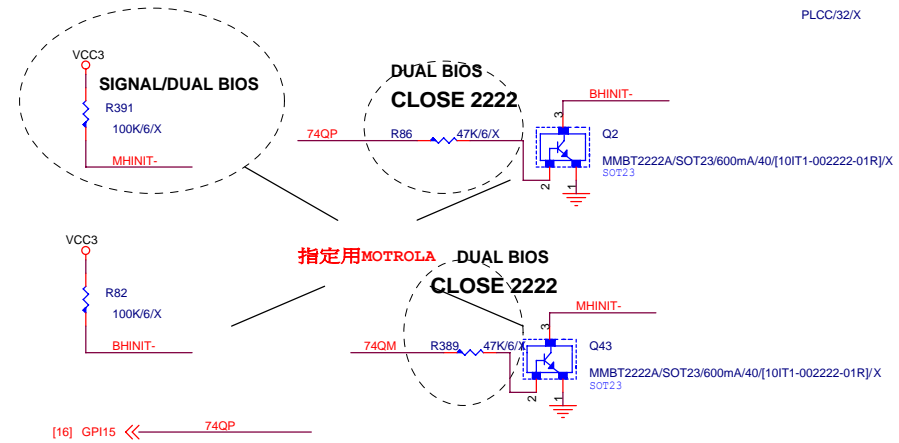
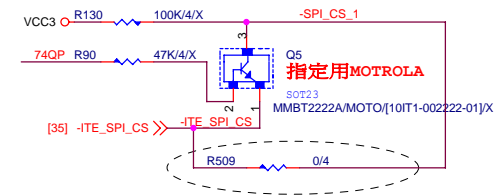
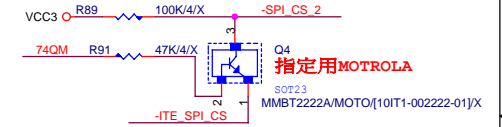
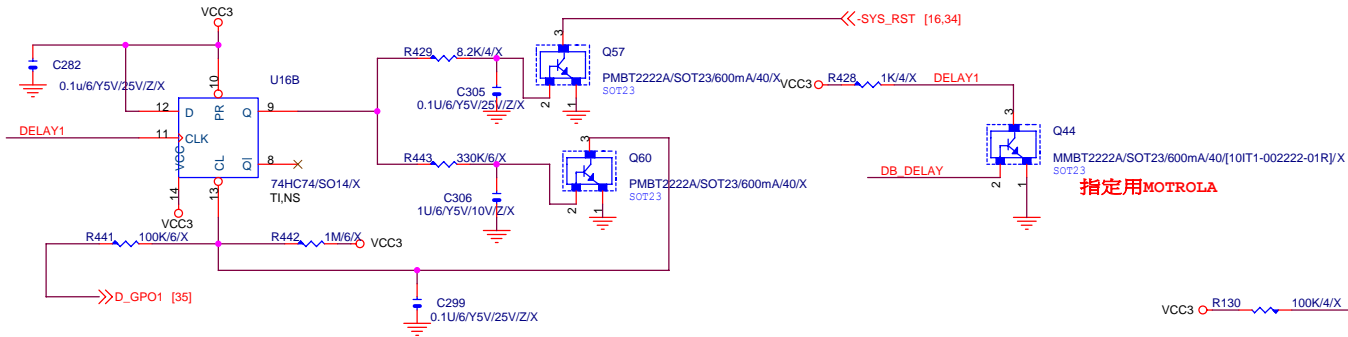
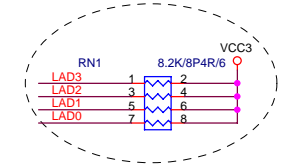
Size	Document Number	Rev
Custom	GA-M57SLI-S4	2.03
Date:	Friday, March 09, 2007	Sheet 31 of 41

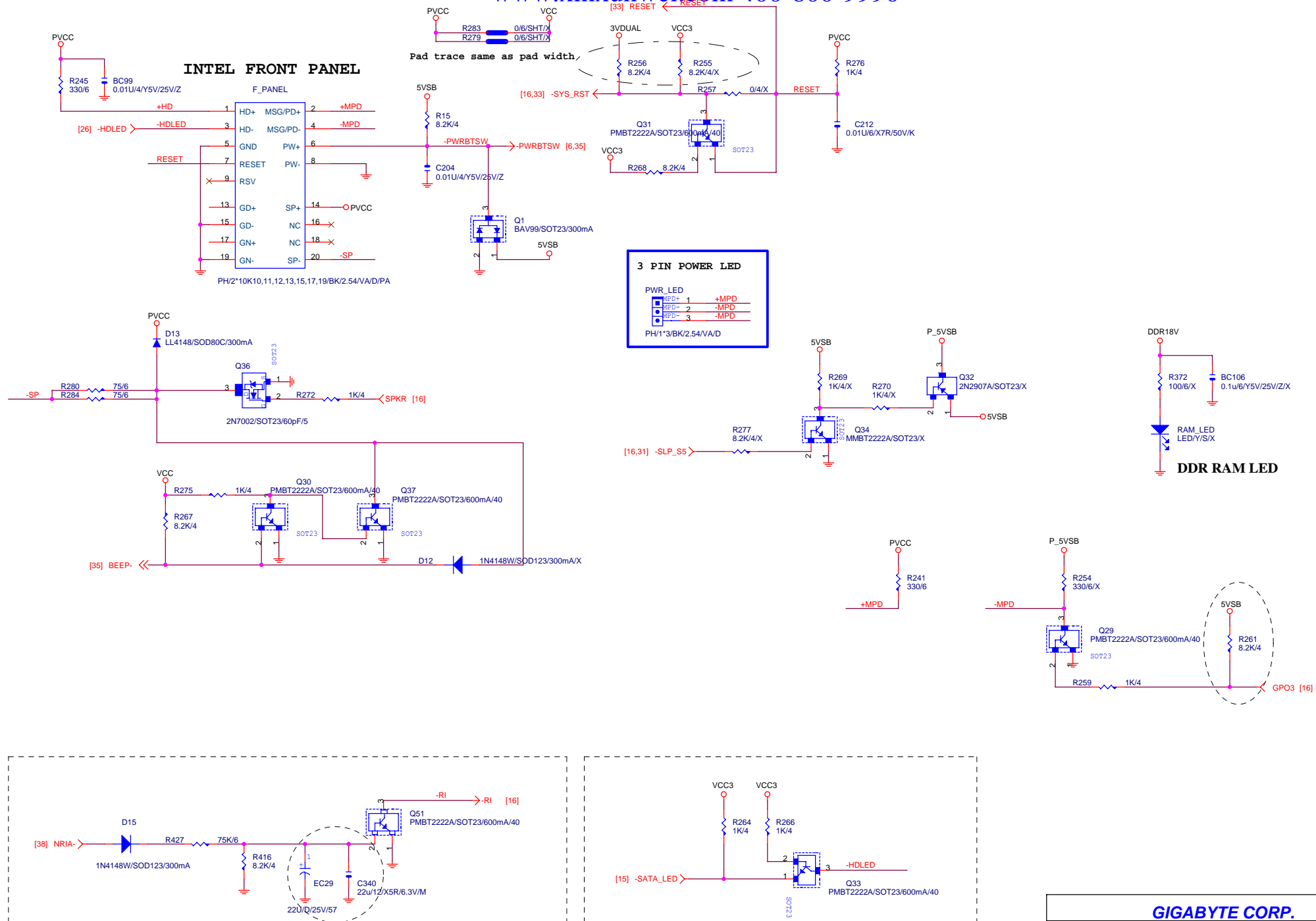
ATX POWER CONNECTOR

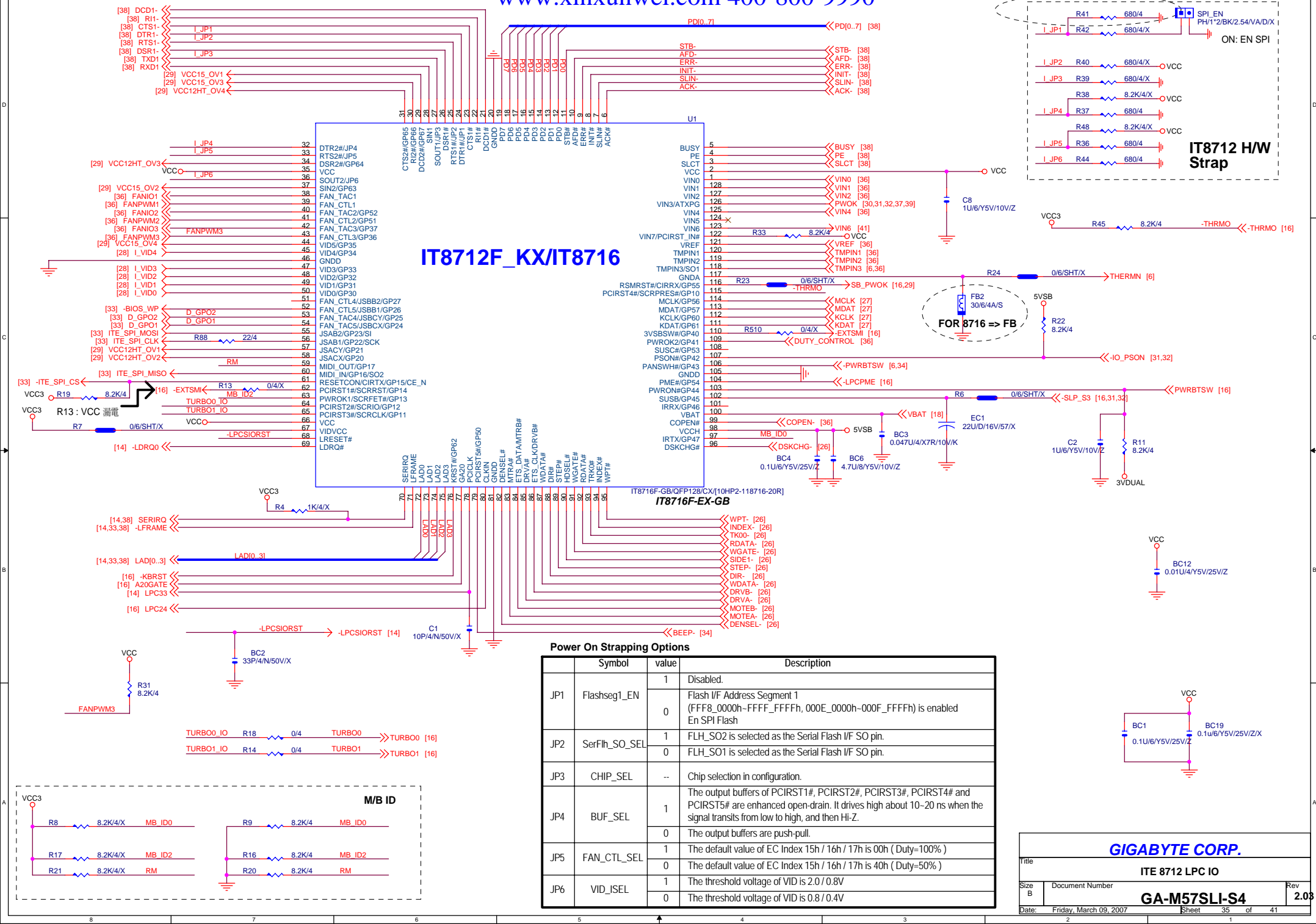




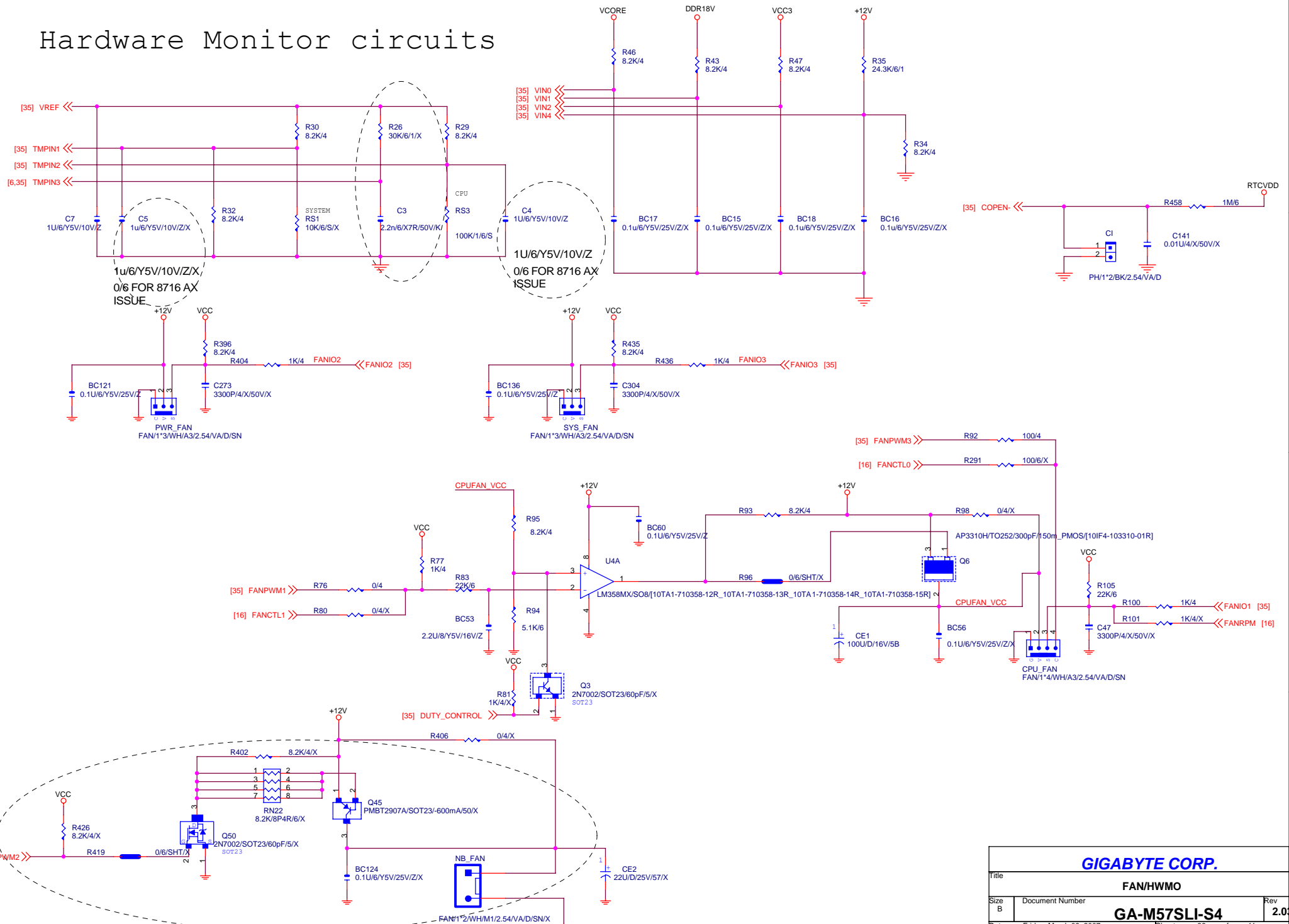
	Main	Backup
GPO30	0	1
GPO28	1	0







Hardware Monitor circuits



GIGABYTE CORP.

FAN/HWMO

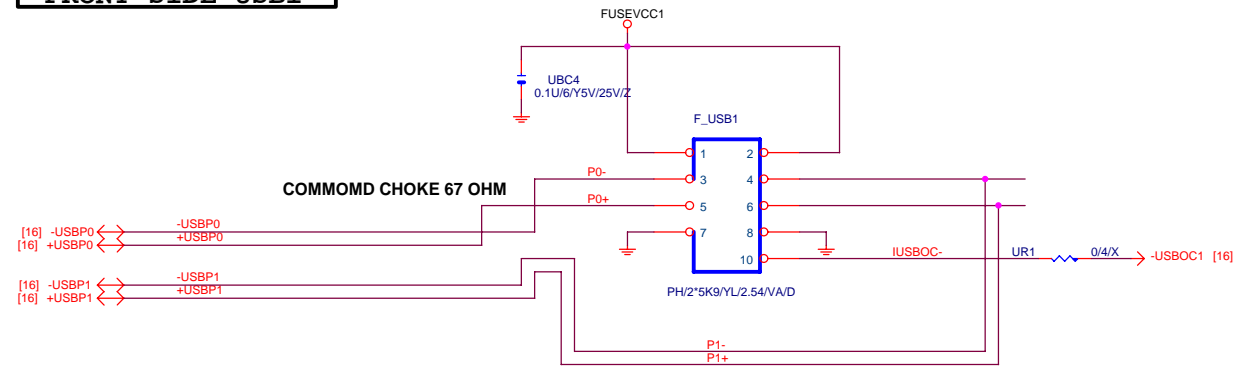
GA-M57SLI-S4

Rev 2.03

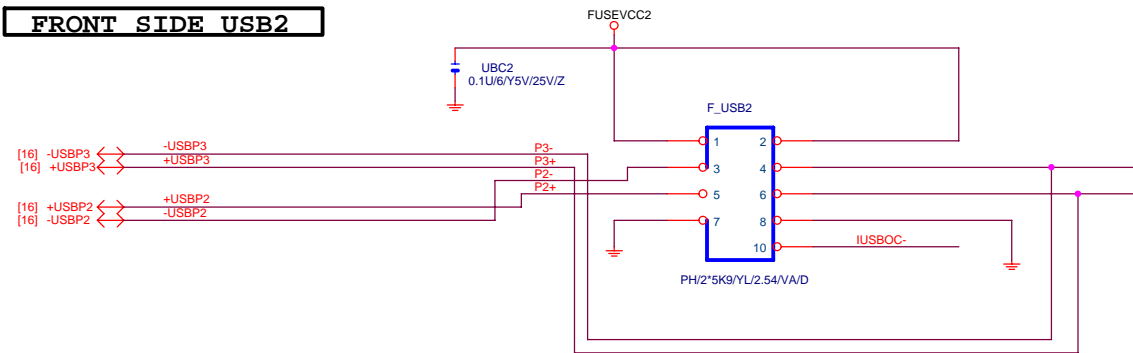
Date: Friday, March 09, 2007

Sheet 36 of 41

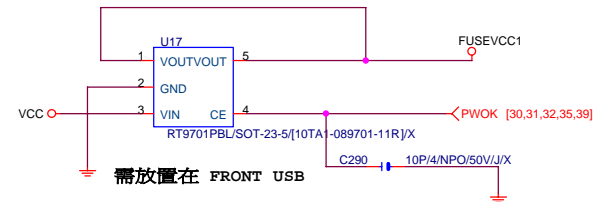
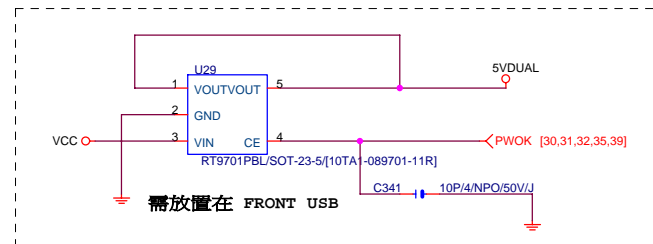
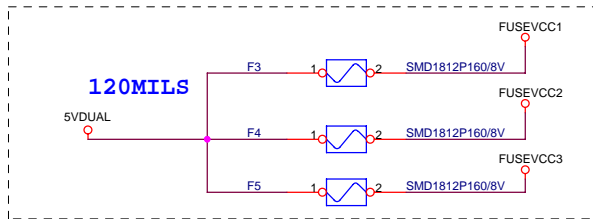
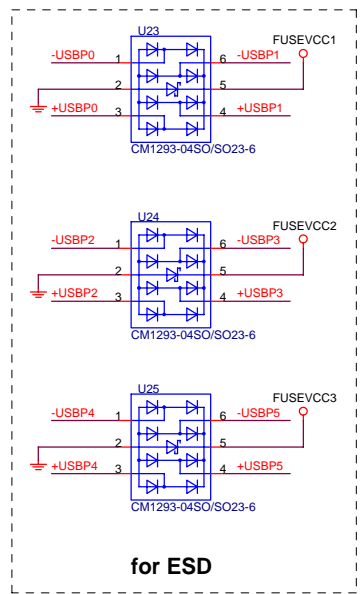
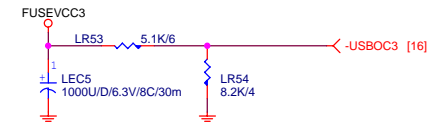
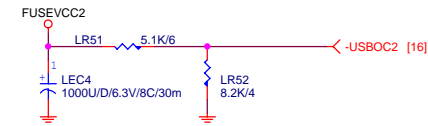
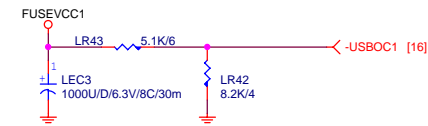
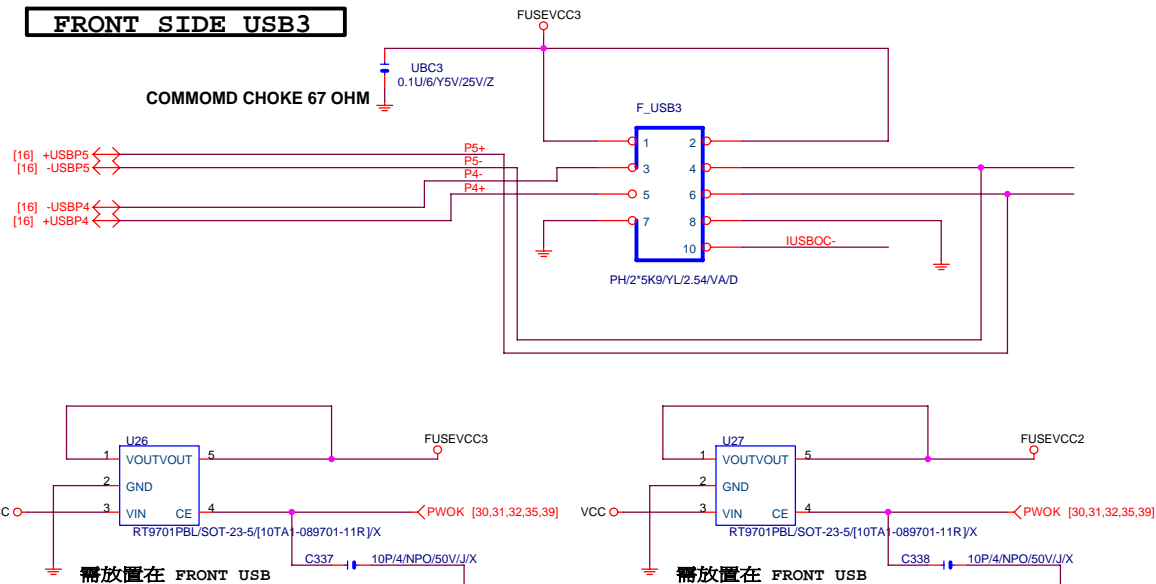
FRONT SIDE USB1



FRONT SIDE USB2

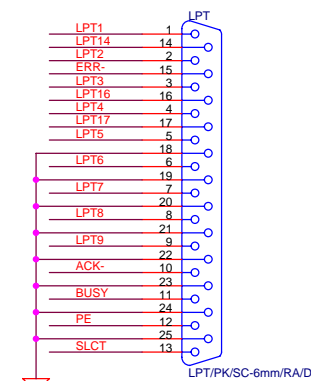
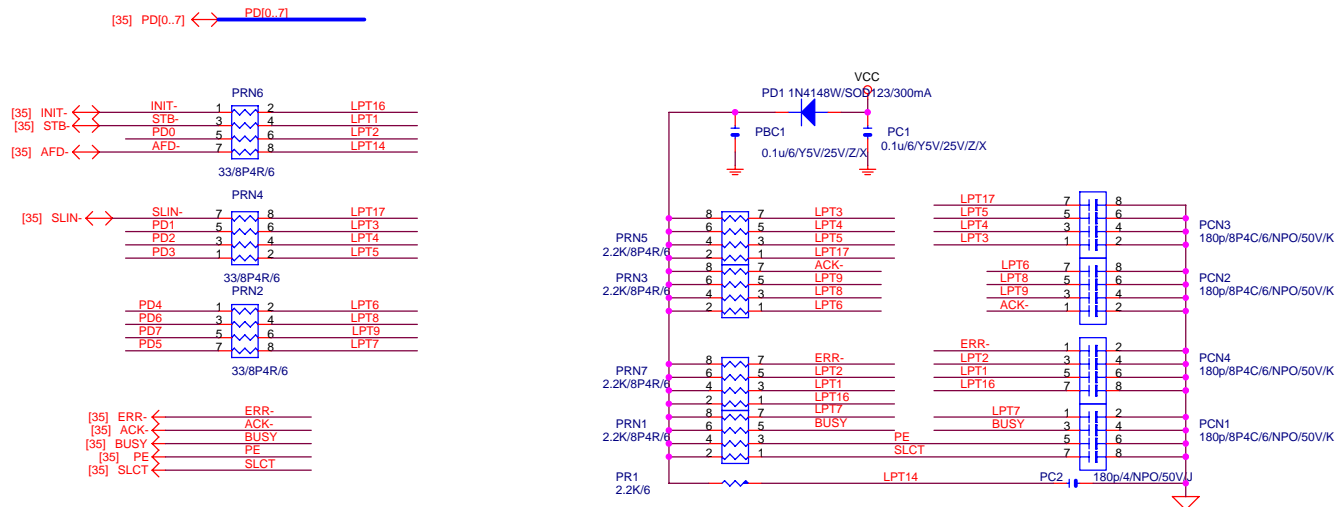
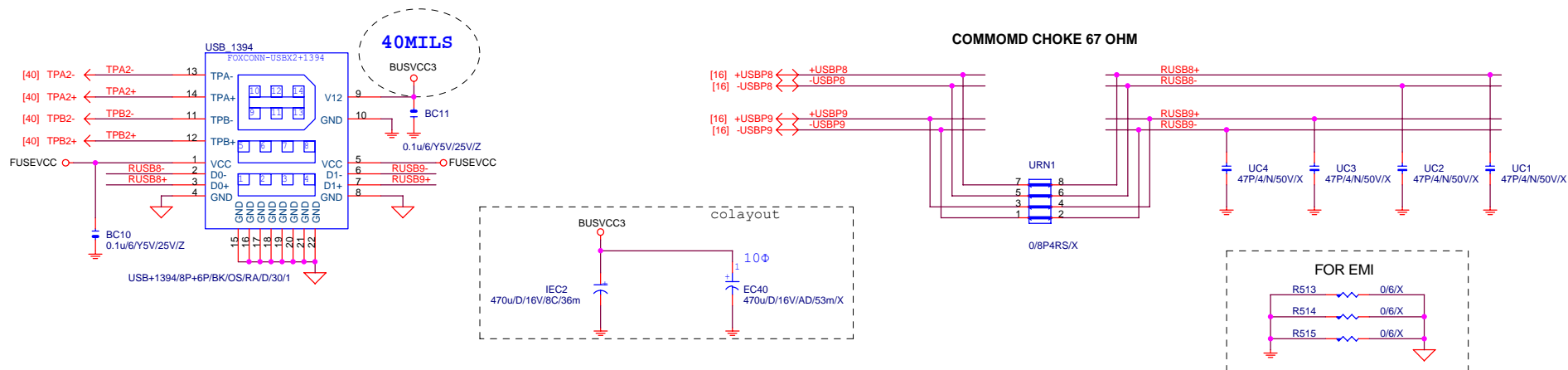
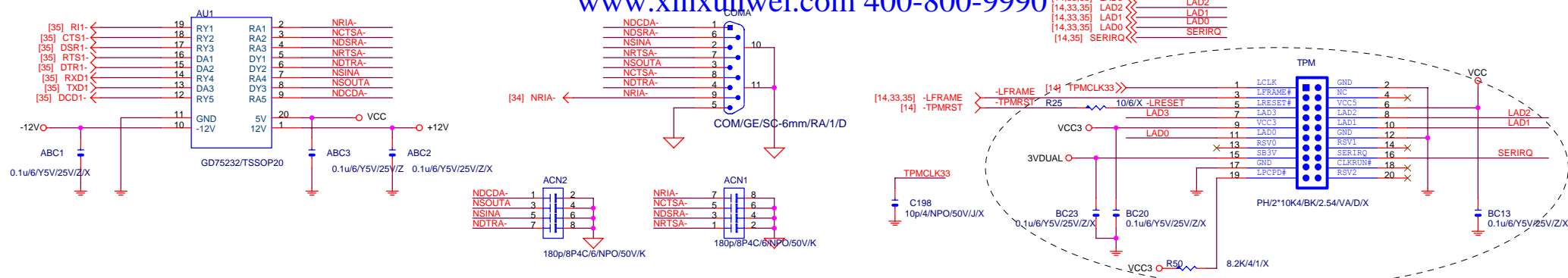


FRONT SIDE USB3



GIGABYTE CORP.

Title			USB PORT
Size	Document Number	Rev	
B		GA-M57SLI-S4	
Date:	Sheet	37 of 41	2.03

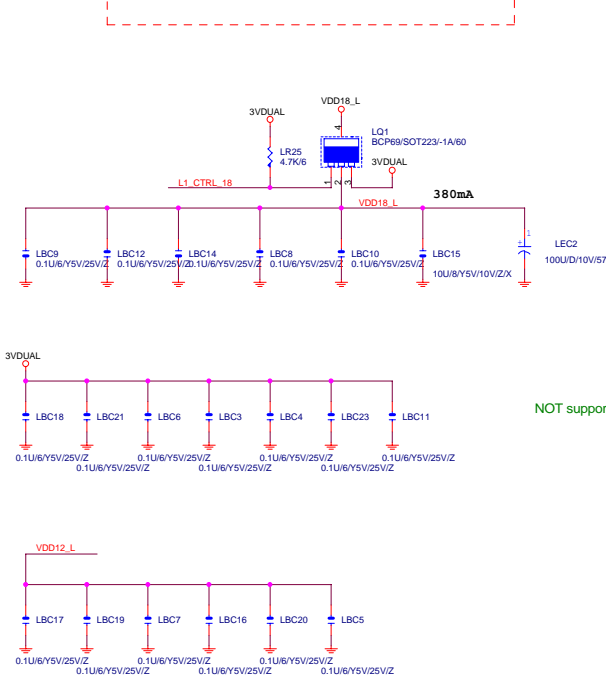


GIGABYTE CORP.

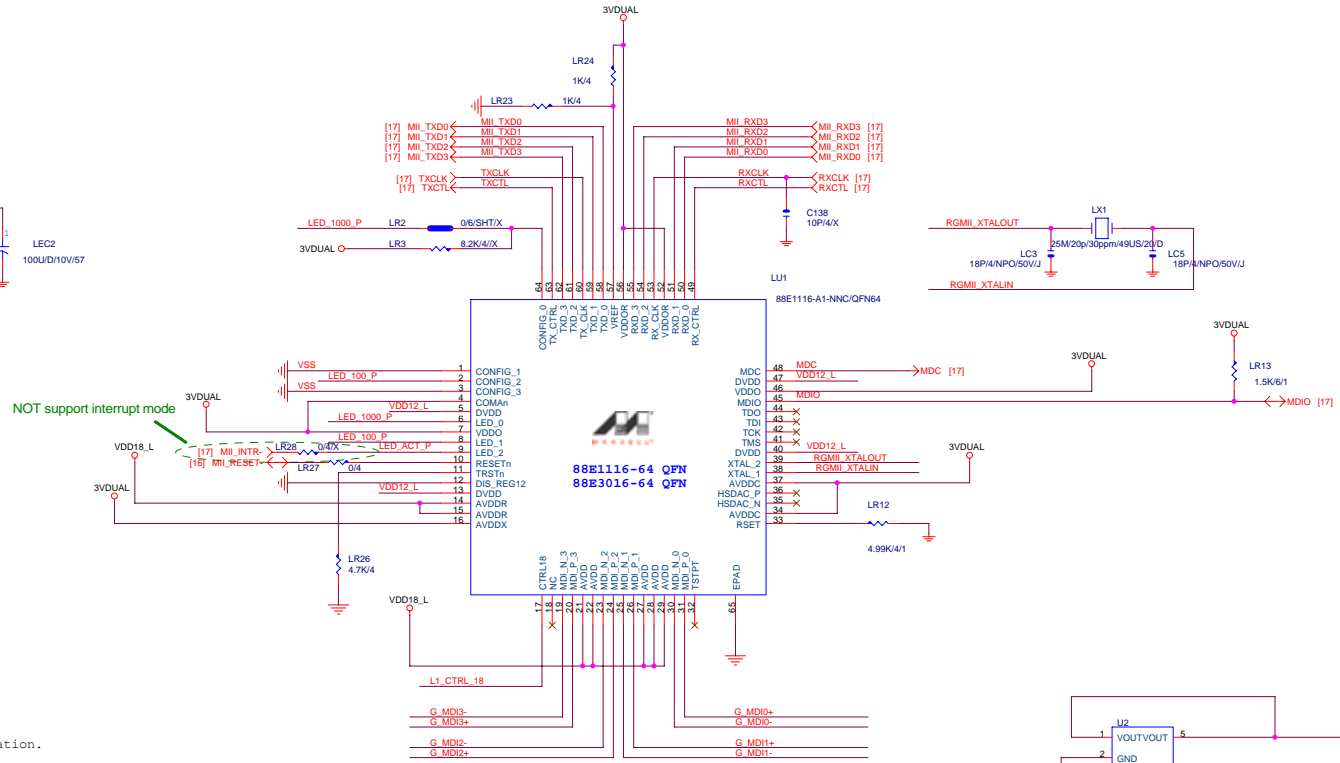
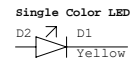
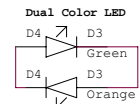
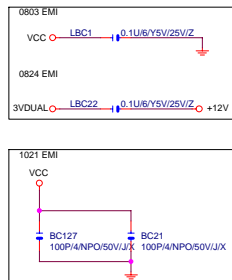
Title			
COM & IR & LPT PORT			
Size	Document Number	Rev	
B	GA-M57SLI-S4	2.03	
Date:	Friday, March 09, 2007	Sheet	38 of 41

El1116 use external 2.5V single power supply.
1.8V create by PNP and 1.2V use internal reg.

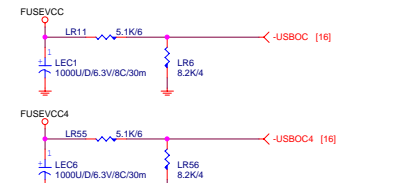
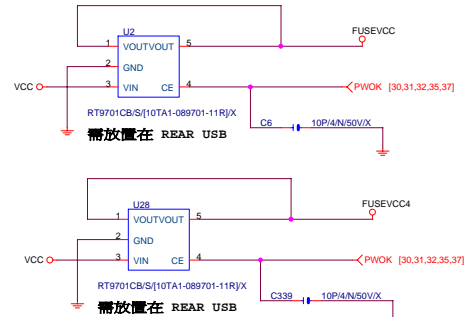
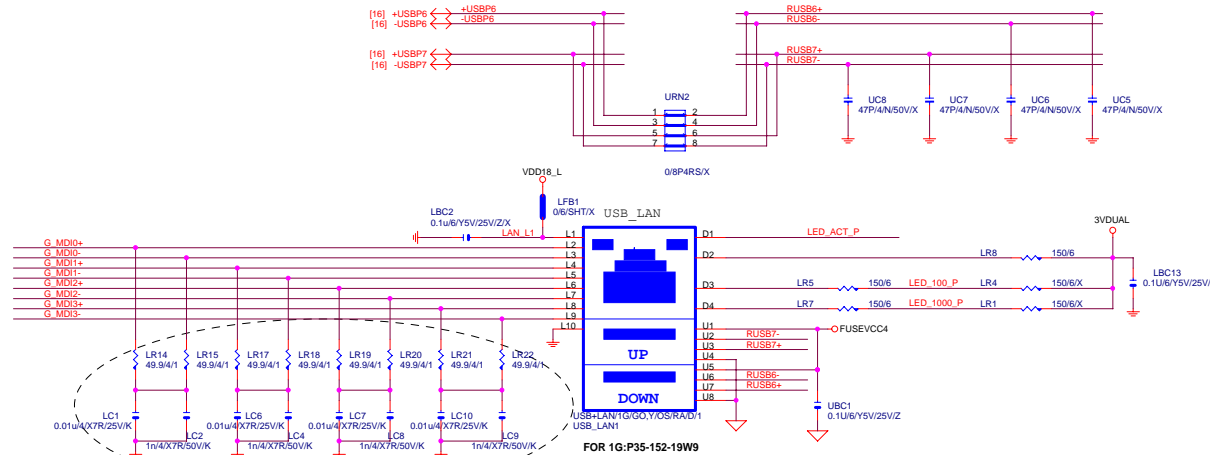
1. PHY address:00001
2. ENA_XC:Enable Auto-Crossover
3. RGMII_TX:Transmit clock not internally delayed
4. RGMII_RX:Receive clock transition when data transitions
5. Advertise all capabilities



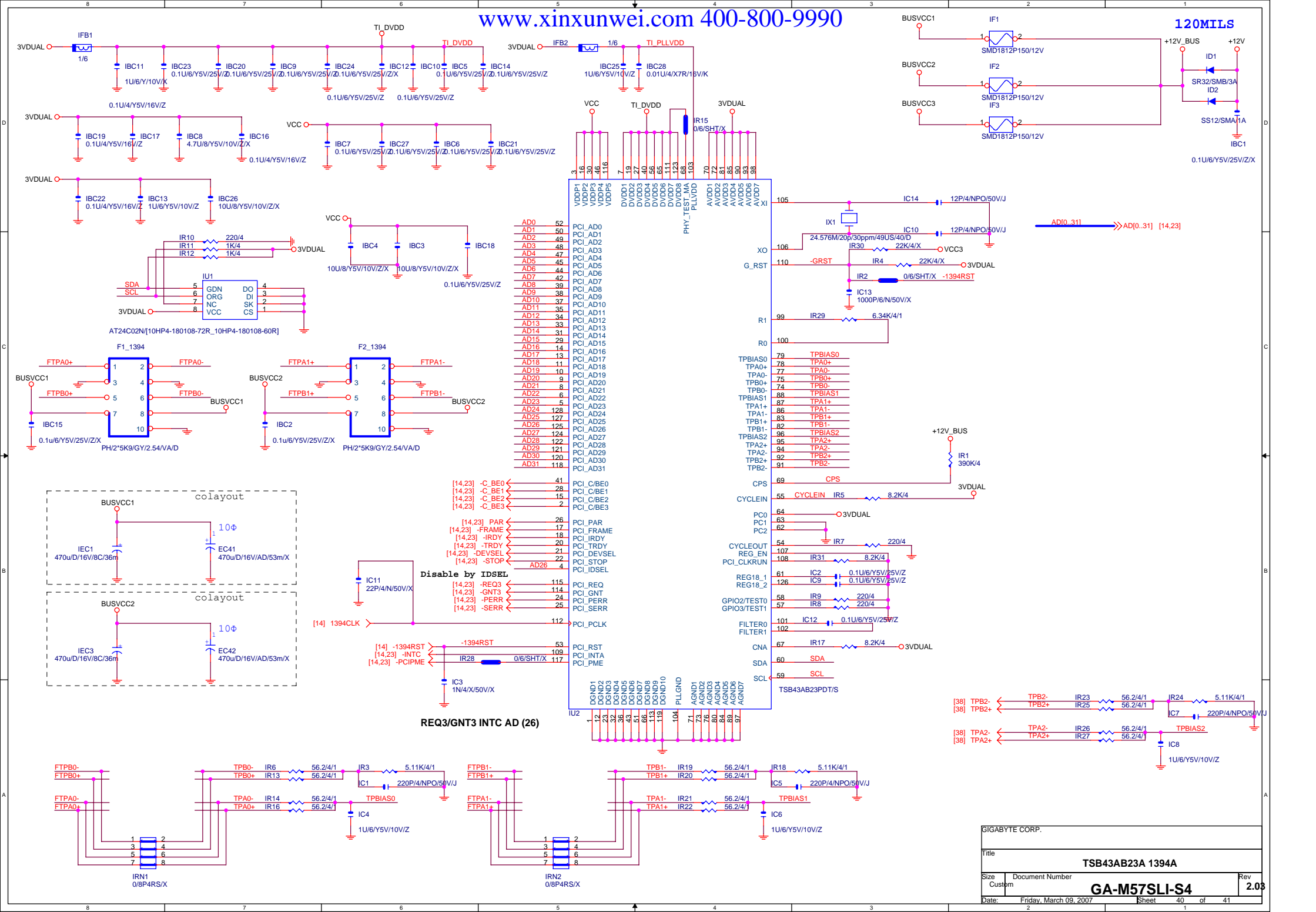
Bypass cap can share. User check it by layout consideration.

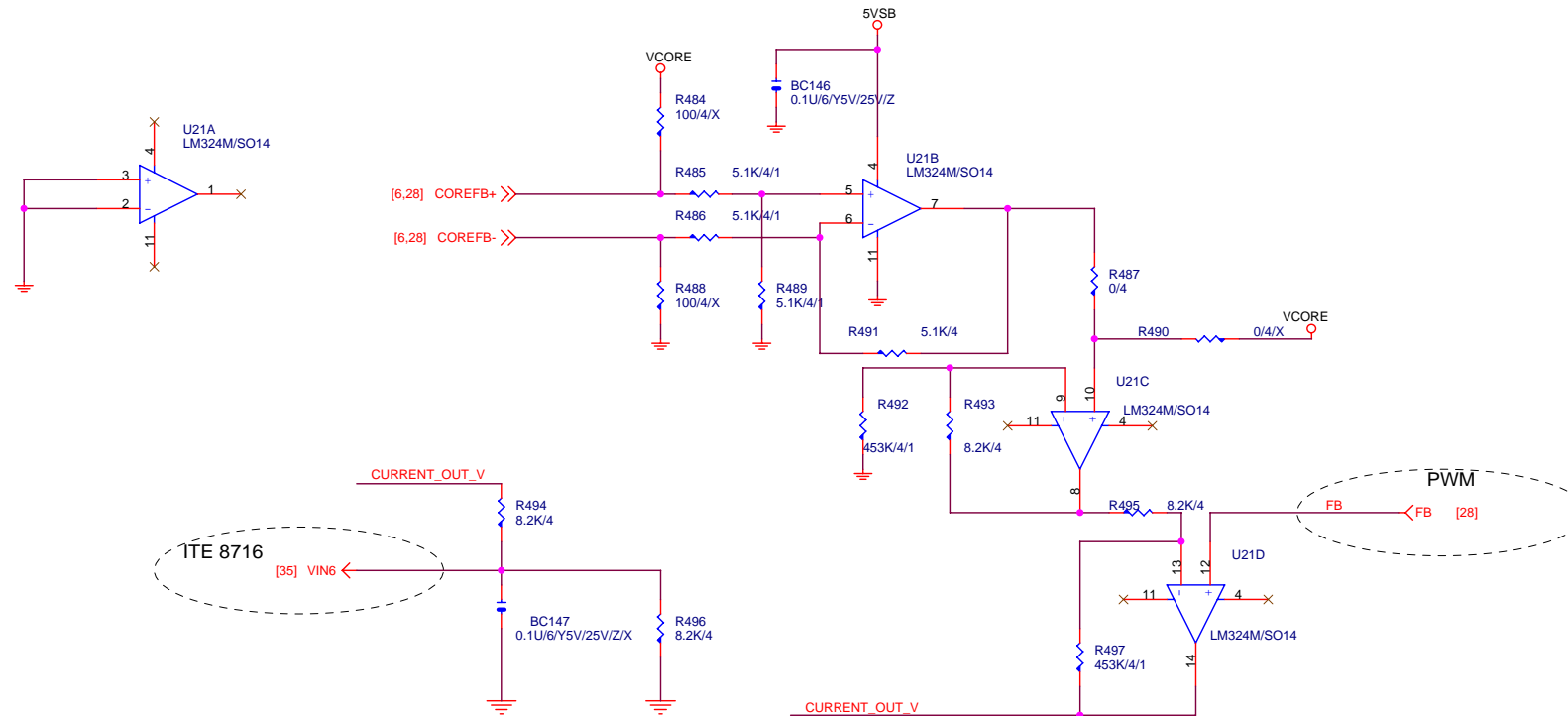


COMMOMD CHOKE 67 OHM



File	Marvell_88E1115_88E1116_88E3016		
Size	Document Number	GA-M57SLI-S4	
C		Rev 2.03	
Date	Friday, March 06, 2009	Sheet	39 of 41



**GIGABYTE CORP.**Title
CURRENT_OUTSize
B Document Number
GA-M57SLI-S4Date: Friday, March 09, 2007 Sheet 41 of 41 Rev
2.03